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Stead-State and Small-Signal Modeling of Power-Stage of PWM Z-Source Converter

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STEADY-STATE AND SMALL-SIGNAL MODELING OF THE POWER-STAGE OF PWM Z-SOURCE CONVERTER

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Doctor of Philosophy

By

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I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Veda Prakash Galigekere N ENTITLED Steady-State and Small-Signal Modeling of the Power-Stage of PWM Z-Source Converter BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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Abstract

Veda Prakash, Galigekere. Ph.D., Engineering Ph.D. Program, Wright State University, 2012. *Steady-State and Small-signal Modeling of Power-Stage of PWM Z-source Converter.*

Pulse-width modulated (PWM) Z-source converter plays an important role in industrial/power electronic systems. Steady-state and dynamic modeling of the power-stage of PWM converters is essential for envisaging a closed-loop regulated power supply.

Steady-state analysis of pulse-width modulated (PWM) Z-source dc-dc converter operating in continuous conduction mode (CCM) is presented. Voltage and current waveforms, and their corresponding expressions describing the steady-state operation of the PWM Z-source dc-dc converter have been presented. The input-to-output dc voltage transfer functions, both for ideal and non-ideal PWM Z-source dc-dc converter have been derived. The minimum Z-network inductance required to ensure CCM operation is derived. The voltage ripple due to filter capacitor and its ESR, and their individual effects on the overall output voltage ripple have been derived and analyzed. Expressions for power loss in each of the components of the PWM Z-source dc-dc converter has been determined. Using the expressions derived to determine the power losses, an expression for the overall efficiency of the PWM Z-source dc-dc has been derived. An example PWM Z-source dc-dc converter is considered. A laboratory prototype is built and the theoretical analysis is in good agreement with the experimental results.

Ac small-signal modeling of pulse-width modulated (PWM) Z-source converter in continuous conduction mode (CCM) by circuit-averaging technique is presented. Averaged dc, low-frequency-large-signal, dc, and ac small-signal models of PWM Z-source converter operating in CCM have been presented. Open-loop power-stage

transfer functions corresponding to the capacitor voltage-loop and inductor current-loop are derived. The transfer functions derived take into account the ESRs of the inductors and capacitors. Experimental validation of the derived small-signal models is presented for a laboratory prototype. The theoretical predictions are in good agreement with the experimental results.

Contents

List of Figures

List of Tables

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1 Introduction

1.1 Background

Switched-mode power converters (SMPC) can be broadly classified into DC-DC converters, DC-AC inverters, AC-DC rectifiers, and AC-AC converters or frequency changers. SMPCs are used extensively in power processors that are used extensively in a myriad of fields such as- automotive electronics, industrial electronics, consumer electronics, defense and space applications, power engineering applications etc,. Additionally, alternate energy sources and distributed generation system is gaining a strong foothold in the power sector. Alternate energy sources and energy storage systems require power electronic interface systems to interact with the main grid or to meet dynamic load variations. The role of power electronic systems is to regulate one or more parameters associated with the input power, and safely meet the load requirements. With this aspect, power engineering in general and power electronics specifically has received renewed interest by researchers [1] - [13].

Conventional voltage-source inverter (or current source inverter) is inherently a buck or step-down (boost or step-up) operation. Neither of them can realize both buck and boost operation. This is a conceptual drawback of voltage-source or current-source inverters [3]-[6]. Z-source inverter presented in [6], overcame the conceptual road-block by presenting a single-stage buck-boost dc-ac inversion mechanism. The Z-source inverter employs a unique impedance network at the source side and hence the name Z-source inverter. Z-source inverter has received significant attention from the academia and the industry [6]-[16].

This dissertation is divided into two parts, they are

1. Detailed steady-state analysis of PWM Z-source dc-dc converter for steady state
2. Small-signal modeling of open-loop power-stage of PWM Z-source converter operating in CCM by circuit-averaging technique

1.2 Steady-State Analysis of PWM Z-source dc-dc converter

This part specifically deals with the dc-dc converter mode of operation of the PWM Z-source converter. A quasi-Z-source based isolated dc/dc converter is presented in [17]. Quasi-Z-source based dc-dc converter [17] utilizes an altered impedance or Z-network derived from the impedance network utilized in the original Z-source inverter of [6]. The authors in [19] and [18] present a brief analysis of a loss-less Z-source dc-dc converter aided by simulation results. The authors in [20] explore the double input version of the PWM Z-source dc-dc converter. The authors in [15] present a brief analysis of a loss-less Z-source dc-dc converter in discontinuous conduction mode and the simulation results. The motivation of this paper is to explore the steady-state operation of PWM Z-source converter in CCM in a more elaborate manner, and to present output voltage ripple analysis of the PWM Z-source dc-dc converter. This work is also published in [21].

Additionally, there has been a renewed interest in isolated and non-isolated voltage step-up PWM dc-dc converters for renewable energy and distributed power generation systems [17]-[27]. Typically, the low output voltage energy source, like fuel-cells requires a PWM dc-dc converter to (1) provide a voltage boost and (2) act as a protective buffer between the load and the energy source. Compared to the conventional boost converter, the PWM Z-source dc-dc converter has a higher input-to-output dc voltage boost factor for the same duty ratio, isolates the source and the load in case of a short-circuit at the load side, and has a second-order output filter. This makes PWM Z-source dc-dc converter a potential topology candidate for renewable energy applications. These features prompt the necessity for a detailed investigation of the steady-state behavior of the PWM Z-source dc-dc converter in CCM.

1.3 Small-Signal Modeling of PWM Z-Source Converter

Power stages of PWM converters are nonlinear owing to the presence of at least one transistor and a diode. In order to apply the known knowledge of linear control theory the power stages need to be averaged and linearized [1]. Nonlinear power stages of PWM converters have been averaged by predominantly two methods: the state-space averaging technique [35] and the circuit averaging technique [36] and [1]. Both the methods have been employed extensively in the past with respect to numerous PWM converters [1], [35] - [40].

The process of circuit averaging involves the replacement of the PWM switch model with an equivalent analog model. The analog model can be obtained by employing current- and voltage- controlled sources. Majority of the PWM dc-dc converters have a switching network that consists of a power MOSFET and a diode connected in a manner such that the two devices have a common point. This network has been identified as the PWM switch network [1], [36]-[40]. The Z-Source converter's schematic is such that the MOSFET and the diode do not have a common point and hence the PWM switch can be thought of as a disjoint PWM switch. The circuit averaging technique has been employed extensively to model the joint PWM switch. The present work presents the extension of the circuit averaging technique to average the disjoint PWM switch present in the Z-Source inverter.

Several articles have contributed to the transient modeling of the PWM Z-source inverter. The transient behavior of the Z-source inverter can be segregated into dc-side phenomenon and ac-side phenomenon [31] and [32]. The dc-side phenomenon can be attributed to the unique Z network and the ac-side phenomenon can be attributed to the inverter's three phase switching process. It has been inferred from [31]-[33] that, for the purpose of investigation of the transient behavior due to the Z network, the six-switch inverter circuit and ac load can be replaced by a current source (inductor)

and a switch to emulate the shoot-through state. Furthermore, [32] states that, the transient behavior of the Z-source inverter is predominantly influenced by the Z network and the dc-side phenomenon. Replacing the inverter with a ac load and a switch in the Z-source inverter leads to a simplified Z-source dc-dc converter with an inductive load. This simplified topology will be referred to as the Z-source dc-dc converter or simply as Z-source converter. The motivation of this work is to present the small-signal modeling of PWM Z-source converter by circuit-averaging technique [34].

1.4 Objectives

1.4.1 Steady-State Analysis of PWM Z-source dc-dc converter in steady-state for CCM

The objectives are to present -

1. The equivalent circuits and the associated expressions corresponding to different stages of operation of the PWM Z-source dc-dc converter in CCM

2. The dc input-to-output voltage conversion factor and minimum inductance required to ensure CCM operation.

3. The equations for power losses in the components of the PWM Z-source dc-dc converter and the overall efficiency.

4. The output voltage ripple across the filter capacitor C_f and its ESR r_{C_f}.

5. The experimental results to validate the theoretical analysis.

1.4.2 Steady-State Analysis of PWM Z-source dc-dc converter in steady-state for CCM

The objectives are -

1. To derive the average large-signal, dc, and ac small-signal linear time-invariant model of PWM Z-source converter operating in CCM by circuit-averaging technique.

2. To derive the small-signal input voltage-to-capacitor voltage, input voltage-to-inductor current, control voltage-to-capacitor voltage, and control voltage-to-inductor current transfer functions including the effects of the ESRs of the passive components.

3. To derive the important step responses based on the power stage transfer functions derived.

4. To experimentally validate all the four derived transfer functions.

2 Overview of PWM DC-AC Inverters

2.1 Background

Traditionally power electronic inverters have been categorized as voltage-source (V-source) or current-source (I-source) inverters. The voltage source inverter (VSI) topology is usually preferred over current source inverters (CSI) owing to its higher efficiency and relatively reduced complexity [3] and [4]. The V-source inverter, although it is popularly employed, suffers from the following drawbacks [6]-

1. Voltage source inversion is inherently a buck or step-down operation. It is not possible to obtain an output voltage with magnitude higher than the input DC voltage. If a higher output voltage is required another step-up stage has to be incorporated to the VSI.

2. No two switches of a single leg of the inverter can be in the ON state simultaneously. This makes the VSI topology vulnerable to mis-gating due to EMI. This mandates the insertion of dead time in the gating function of the inverter leading to possible waveform distortion.

The I-source inverter, which is realized by a large inductor fed by a voltage source has the following drawbacks [6]-

1. Current source inversion is inherently a boost or step-up operation. It is not possible to obtain an output voltage with magnitude lesser than the input DC voltage. If a reduced output voltage is required another step-down stage has to be incorporated to the CSI. This increases the complexity of the system.

2. At least one upper level switch and one lower level switch has to be in the ON state at any time instant. If this requirement is not satisfied, the dc inductor would be open circuited and could potentially destroy the devices. As a result,

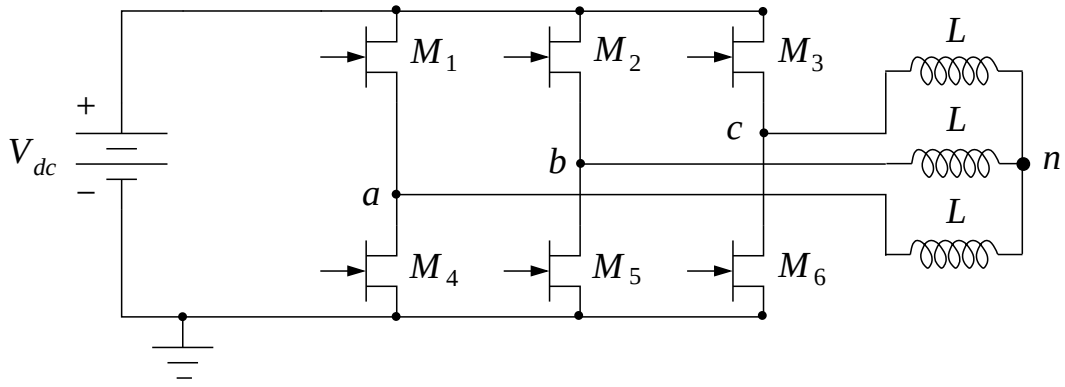

Figure 2.1: Three-leg six-switch voltage source inverter.

contrary to VSI, CSI requires overlapping needs to be inserted into the gating function. This leads to waveform distortion.

2.2 Three-leg Six-Switch PWM DC-AC Inverter

This section presents the overview of the operation of a three-leg six-switch VSI. The operation is described in several articles and reference books [3] and [4]. Three-phase VSI employs a three-leg six-switch network fed by a voltage source as shown in Fig. 2.1 [3] and [4]. The six switches which are typically MOSFETs or IGBTs are switched in a specified sequence based on the modulation technique employed to synthesize the required ac output voltage. The top level switches are denoted as as M_1, M_2, and M_3 and the bottom level switches are M_4, M_5, and M_6. The top switch and the

Switching vector	ON	State	v_{ab}	v_{bc}	v_{ca}
100	1,5,6	active	V_{dc}	0	$-V_{dc}$
110	1,2,6	active	0	V_{dc}	$-V_{dc}$
010	2,4,6	active	$-V_{dc}$	V_{dc}	0
011	2,3,4	active	$-V_{dc}$	0	V_{dc}
001	3,4,5	active	0	$-V_{dc}$	V_{dc}
101	2,3,5	active	V_{dc}	$-V_{dc}$	0
111	1,2,3	zero	0	0	0
000	4,5,6	zero	0	0	0

Table 2.1: Allowable Switching States of a Six-Switch VSI

bottom switch of each leg have complimentary gating functions. Depending on the

state of the 6 switches the VSI has 6 active states and 2 null or zero states [3] and [6]. The 6 active states correspond to a finite voltage appearing across the terminals a, b, and c. The 2 null states correspond to either all the top switches being ON or all the top witches being OFF. The output voltage associated with the null state is 0. The possible state vectors for a conventional VSI is shown in Table 2.1. For a VSI as depicted in Fig. 2.1, If V_{dc} is the input voltage and M is the modulation index, the peak phase voltage is [3] and [4]

$$v_{a(peak)} = M.\frac{V_{dc}}{2}. \tag{2.1}$$

Typically, $M < 1$ as VSIs are usually not operated in the over-modulation zone. From (2.1) it is evident that for a conventional VSI the output voltage is significantly lesser than the input voltage. The value of M depends on the pulse-width modulation scheme employed.

Sinusoidal PWM

Sinusoidal PWM (or Sine-triangle modulation) is one of the popular techniques employed to invert dc to single phase or three phase ac [2] - [3]. In sinusoidal PWM, a high frequency (carrier) triangle wave is continually compared with single phase or three phase reference signal. In this method, the output voltage follows the reference signal. The frequency of the carrier signal decides the switching frequency of the Inverter switches [3] and [4]. Sine-triangle modulation scheme is depicted in Fig. 2.2.

Modulation index M is defined as the ratio of the peak value of the carrier signal to the peak value of the reference signal

$$M = \frac{V_{reference}}{v_{carrier}} = \frac{v_{sine}}{v_{triangle}}. \tag{2.2}$$

For an input dc voltage of 100 V and $M = 0.8$, the peak value of the phase voltage based on (2.1) is

$$v_{a(peak)} = 0.8 \times \frac{100}{2}$$

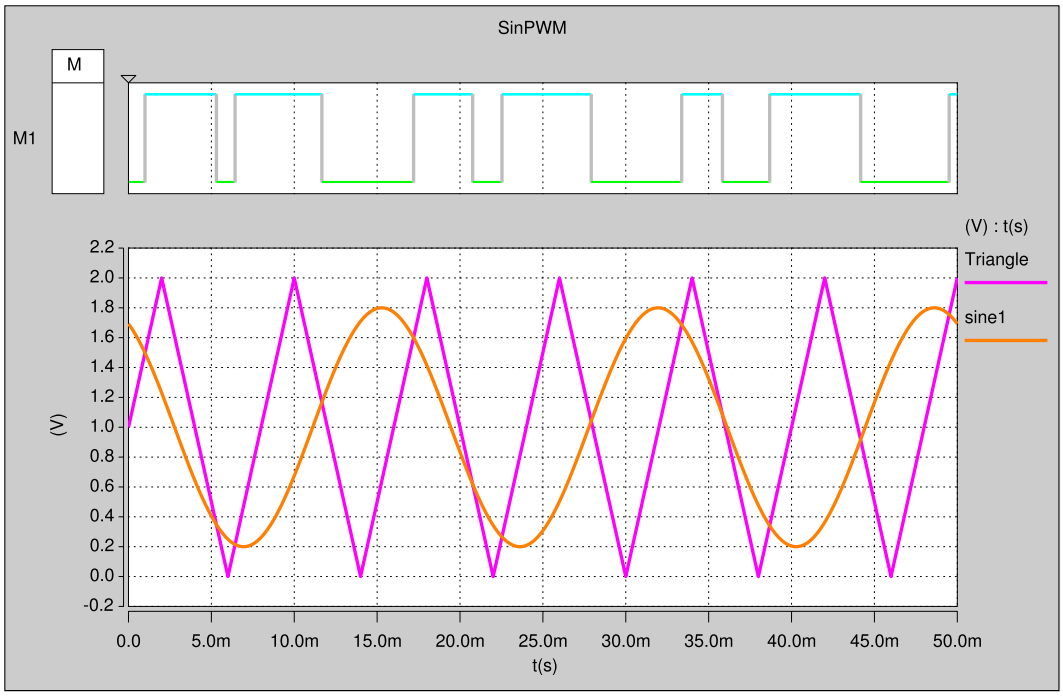

Figure 2.2: Sine-Triangle modulation.

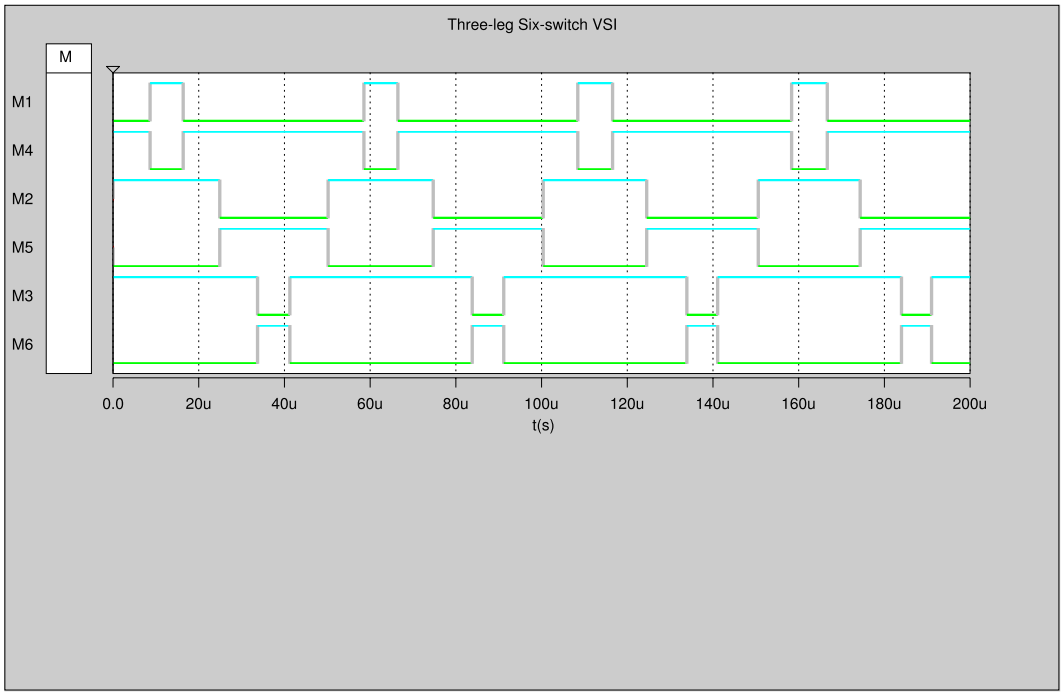

Figure 2.3: Saber Sketch waveforms - Gating functions obtained by sine-triangle modulation.

$$v_{a(peak)} = 40 \text{ V}. \tag{2.3}$$

Three-leg six-switch conventional VSI inverter was simulated in Saber. Ideal semiconductor switches were employed with sine-triangle modulation technique with $M = 0.8$. Sample of the gate pulses obtained by sine-triangle modulation employing Saber is shown in Fig. 2.3. Figure 2.4 shows the key simulation results. It can be inferred from Fig. 2.4 that the simulation results are in good agreement with the predicted value in (2.3).

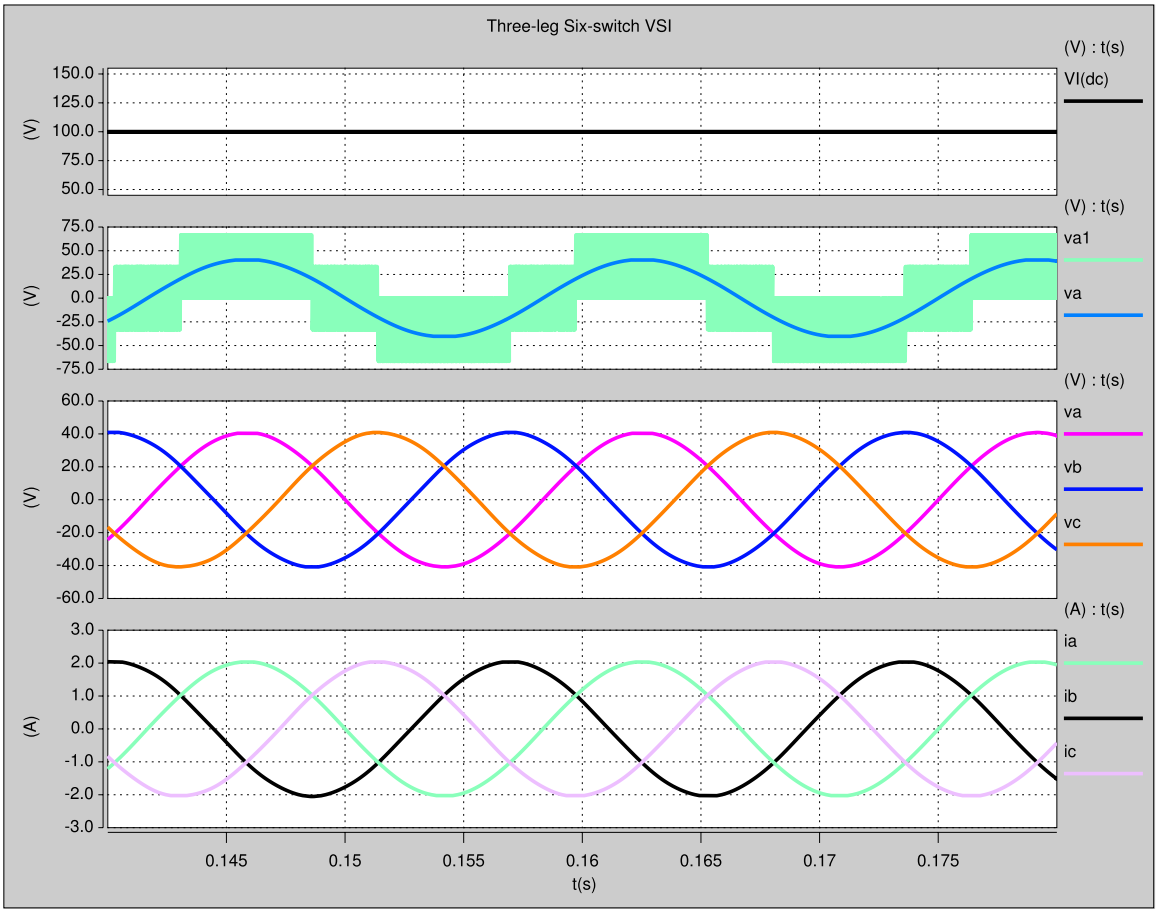

Figure 2.4: Saber Sketch waveforms - Input voltage $V_{I(dc)}$, phase voltage before line filter v_{a1}, phase voltage v_a, three phase voltages $v_{a,b,c}$, and three phase currents $i_{a,b,c}$.

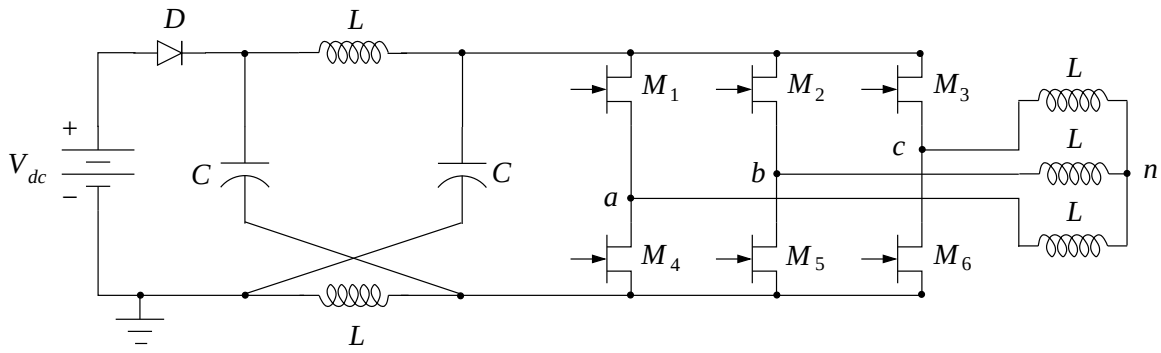

Figure 2.5: Z-source inverter.

2.3 Z-Source or Impedance-fed Inverter

Z-Source Inverter presented in [6] employs a unique impedance network interfacing the DC source and the six switch inverter network as shown in Fig. 2.5. The Z-Source inverter has the ability to either buck or boost the input DC voltage while retaining the voltage inversion capability. As a consequence of employing the Z impedance network, an additional state in which either one or more of the inverter legs can be shorted for a finite time duration is feasible. This state is termed as the shoot-through state [6]. The shoot-through zero state and the Z network incorporate the voltage boost or the voltage step-up feature to the Z-Source converter. The shoot-through state can be achieved by shorting any one phase leg, or shorting combinations of two phase legs, or by shorting all the three legs. The shoot-through state which emulates the behavior of the boost topology is forbidden in conventional VSIs and CSIs. Since the shoot-through state is a zero state, the Z-source inverter retains all the PWM features associated with the VSI. The possible state vectors for Z-source converter are shown in Table 2.2 [6] - [10]. Simple extension of the sine-triangle modulation leads to a reliable constant-boost technique for Z-Source inverter [10]. In this scheme along with the sinusoidal signal, two reference dc signals are employed to obtain the shoot-through pulses. The sinusoidal signal and the reference dc signals are compared to the same triangular carrier signal. The reference dc signal should be higher than

Switches ON	State
1,2,3,4,5,6	shoot-through zero state
1,2,4,5	shoot-through zero state
1,3,4,6	shoot-through zero state
2,3,5,6	shoot-through zero state
1,4	shoot-through zero state
2,5	shoot-through zero state
3,6	shoot-through zero state

Table 2.2: Possible switching combinations to realize the shoot-through state

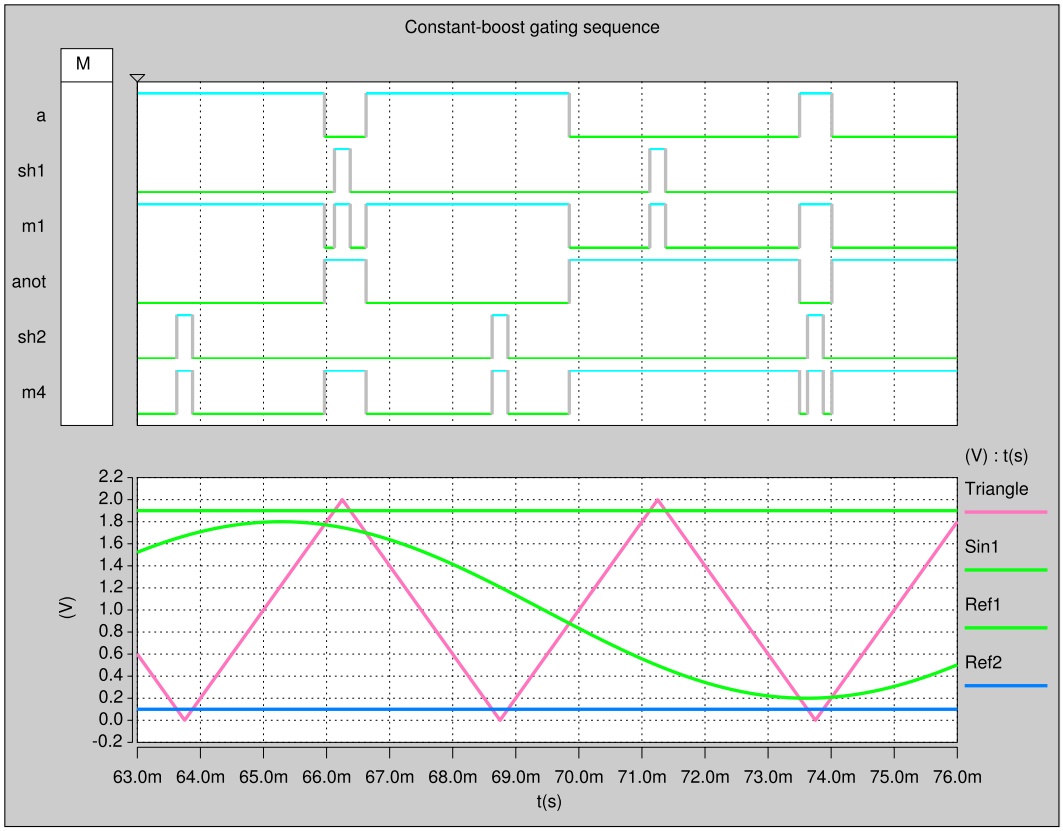

Figure 2.6: Constant boost pulse-width modulation scheme for Z-source inverter.

the amplitude of the sinusoidal signal but within the range of the triangular signal. The constant boost method is depicted in Fig. 2.6. In the Fig. 2.6, a is obtained by comparing the sinusoidal wave and the triangle wave and a is inverted to obtain a_{not}, sh_1 and sh_2 are obtained by comparing the dc reference signals and the triangle signal. a and a_{not} are logically OR with sh_1 and sh_2 to obtain the gate pulses M_1 and M_4 respectively. If T_{sh} is the shoot-through time duration for one switching time

period T,the peak phase voltage of Z-source inverter is given by

$$v_{a(peak)} = MB\frac{V_{dc}}{2}, \tag{2.4}$$

where

$$B = \frac{1}{1 - 2\frac{T_{sh}}{T}}. \tag{2.5}$$

For an input dc voltage of $V_{dc} = 100$ V and modulation index $M = 0.8$, B required to obtain an output peak voltage of $v_{a(peak)} = 150$ V is calculated, as per 2.4 to be 3.75. For a switching time period $T = 50$ μs, the shoot-through time per period is calculated using (2.5) to be 18.3 μs. A Z-source inverter was simulated in Saber with Z network inductors and capacitors being $L_1 = L_2 = L = 160$ μH and $C_1 = C_2 = C = 1600$ μH. The Z network inductor and capacitor values are obtained based on relevant literature [6]. Figure 2.7 shows the key waveforms associated with the Z-source inverter. The simulation results validate (2.4) and (2.5).

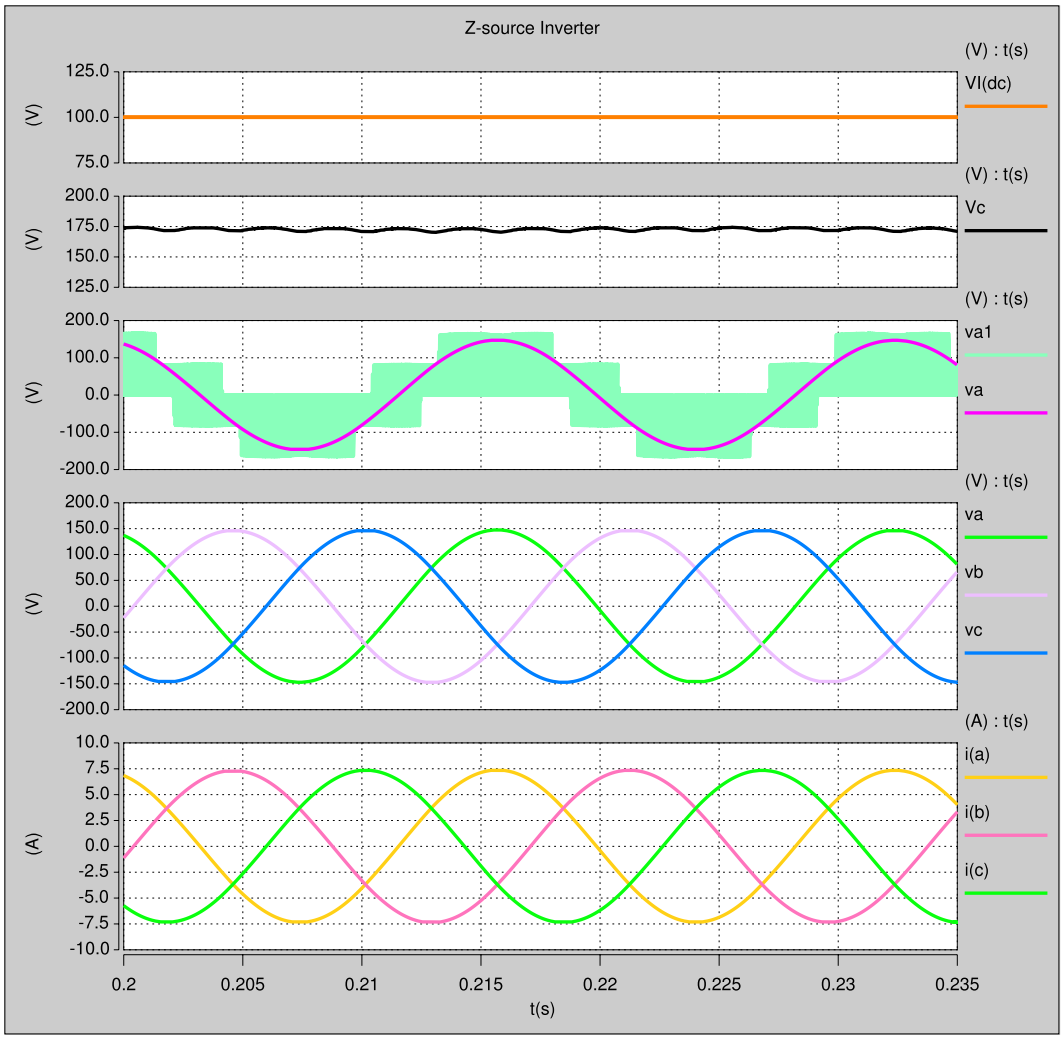

Figure 2.7: Saber Sketch waveforms - key waveforms of Z-source inverter.

3 Small-Signal Modeling of PWM Z-source Converter by Circuit-Averaging Technique

3.1 Introduction

State-space averaging [35] and circuit-averaging [36] methods have been two of the popular methods for obtaining small-signal models of PWM power converters. The state-space averaging technique involves the averaging of the state equations associated with the different switching states of a converter. In the circuit-averaging technique, the averaging is performed on the switching component waveforms. The circuit-averaging technique tends to give a better physical insight into the circuit behavior. The primary aspect in the circuit-averaging technique is to replace the nonlinear switching network of the converter by an equivalent averaged and linearized network [1] and [2], [34].

Authors in [31] and [32] elaborate on the ac-side phenomenon and the dc-side phenomenon of the Z-source inverter, and show the presence of a right-half-plane zero in the control-to-output transfer function by the state-space averaging and signal-flow-graph analyses. In [31] and [32], the dc-side phenomenon of the Z-source inverter is studied using state-space averaging based small-signal analysis and signal-flow-graph analysis, and the ac-side phenomenon is studied in detail by using the space vector analysis. Authors in [33] have presented the small-signal modeling of the PWM Z-source converter by state-space averaging technique. They present the open-loop power stage small-signal input voltage-to-capacitor voltage, input voltage-to-inductor current, control voltage-to-capacitor voltage, and control voltage-to-inductor current transfer functions for the PWM Z-source converter in CCM. Authors in [33] also elaborate on the design-oriented analysis for the Z-source converter operating in CCM. However, the small-signal model and the transfer-functions do not take into account the ESRs of the capacitors and the inductors. This limits the accuracy of

the model in the frequency range where the ESRs can play a dominant role. This section presents the small-signal modeling of the PWM Z-source converter operating in CCM by circuit-averaging technique.

3.2 DC Analysis of PWM Z-source Converter

The transient behavior of the Z-source inverter can be segregated into dc-side phenomenon and ac-side phenomenon [32]. The dc-side phenomenon can be attributed to the unique Z network and the ac-side phenomenon can be attributed to the inverter's three phase switching process. It has been inferred from [31] - [33] that, for the purpose of investigation of the transient behavior due to the Z network, the six-switch inverter circuit and ac load can be replaced by a current source (inductor) and a switch to emulate the shoot-through state. Furthermore, [32] states that, the transient behavior of the Z-source inverter is predominantly influenced by the Z network and the dc-side phenomenon. Replacing the inverter with a ac load and a switch in the Z-source inverter leads to a simplified Z-source dc-dc converter with an inductive load. This simplified topology will be referred to as the Z-source dc-dc converter or simply as Z-source converter.

This section presents the basic steady state analysis of a PWM Z-source converter based on [6], [31] - [33]. Steady state analysis has been carried out to obtain the necessary expressions required for small-signal modeling of the Z-source converter. Parameters of particular interest are the current through the switch S, and the voltage across the diode D. The analysis assumes the Z-source converter to be operating in the continuous conduction mode.

3.3 Assumptions

Based on the analysis in [1], The following assumptions have been made:

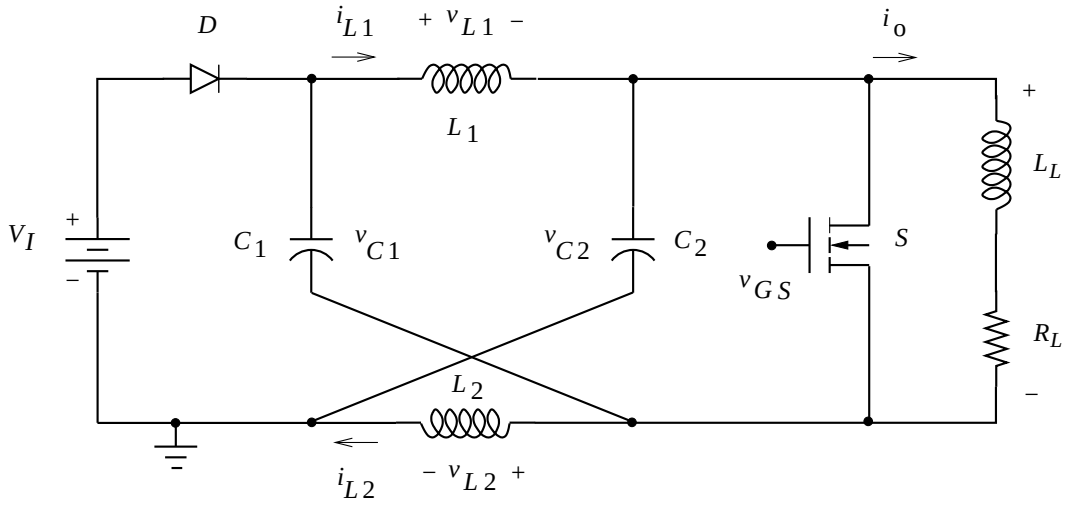

Figure 3.1: PWM Z-source dc-dc Converter.

1. The output capacitance of the transistor and the junction capacitance of the diode have been neglected.

2. Inductors, capacitors and resistors are assumed to be linear, time-invariant and frequency independent.

3. The on-state resistance of the transistor is linear and the off-state resistance is infinity.

4. The diode is represented by a linear battery and a forward resistance in the on-state and by infinite resistance in the off-state.

5. Storage-time modulation of the transistor is neglected.

3.4 Steady State Analysis of PWM Z-source Converter for CCM

A PWM Z-source converter is depicted in Fig. 3.1. It consists of a diode D (uncontrolled switch), a MOSFET S (controlled switch), two inductors L_1 and L_2 and two capacitors C_1 and C_2 connected in a manner to obtain the Z network, and an ac load consisting of a load or output inductor L_L and a load or output resistor R_L connected

in series. The switch S is switched at a constant switching frequency $f_S = 1/T$ and the duty cycle is defined as

$$D = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}}, \tag{3.1}$$

where t_{on} is the time duration when the switch S is ON and t_{off} is the time duration when the switch S is OFF. As is the case with most of the PWM converters the switches S and D are ON or OFF in a complimentary manner.

3.4.1 Time Interval $0 \leq t \leq DT$

The equivalent circuit representing the stage when the switch S is ON and the diode D is OFF is depicted in Fig. 3.2. This state encompasses the shoot-through state of the Z-source inverter. In this state the supply is isolated from the load. At $t = 0$, the switch S turns ON and due to the existing circuit conditions the diode D is reverse biased and is OFF. Envisaging $C_1 = C_2 = C$ and $L_1 = L_2 = L$, and due to the

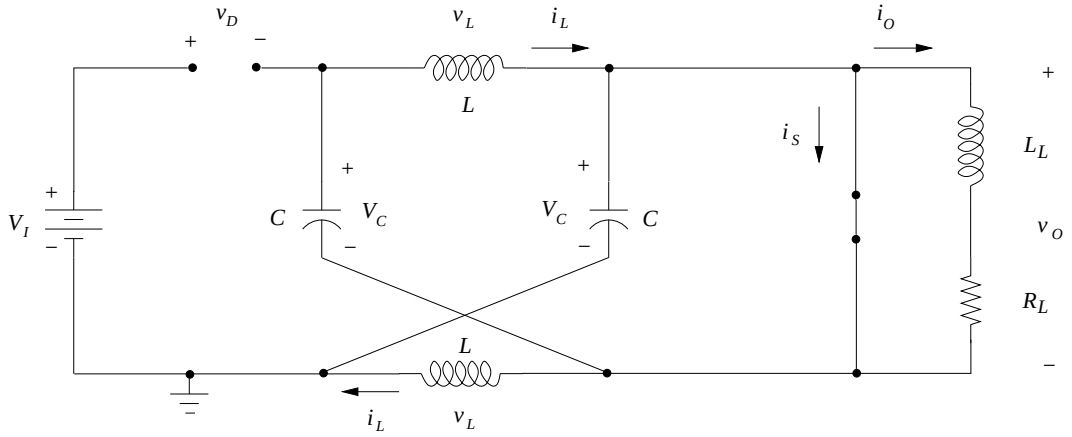

Figure 3.2: Equivalent circuit of the PWM Z-source converter when the switch is ON and the diode is OFF.

symmetry of the Z network

$$v_{C1} = v_{C2} = V_C \tag{3.2}$$

and

$$v_{L1} = v_{L2} = v_L \text{ and } i_{L1} = i_{L2} = i_L. \tag{3.3}$$

The voltage (anode to cathode) across the diode D in this stage is

$$v_D = V_I - 2V_C. \tag{3.4}$$

The voltage across the Z network inductor is

$$v_L = 2V_C - V_C = V_C = L\frac{di_L}{dt}. \tag{3.5}$$

Hence, the current through the inductor is given by

$$i_L = \frac{1}{L}\int_0^t v_L dt + i_L(0) = \frac{V_C}{L}\int_0^t dt + i_L(0) \tag{3.6}$$

where $i_L(0)$ is the initial current in the inductor at time $t = 0$. The peak inductor current is given by

$$i_L(DT) = \frac{V_C}{L}(DT) + i_L(0) \tag{3.7}$$

and the peak-to-peak inductor current ripple is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_C}{L}DT = \frac{DV_C}{f_S L}. \tag{3.8}$$

By Kirchoff's current law, the current through the switch is

$$i_S = 2i_L - i_O. \tag{3.9}$$

3.4.2 Time Interval $DT \leq t \leq T$

In this stage the switch S is OFF and the diode D is ON. The Z network acts as the interface between the load and the source. Equivalent circuit representing this stage is depicted in Fig. 3.3. The voltage across the inductor is

$$v_L = V_I - V_C = L\frac{di_L}{dt}. \tag{3.10}$$

The current through the inductor is

$$i_L = \frac{1}{L}\int_{DT}^t v_L dt + i_L(DT)$$

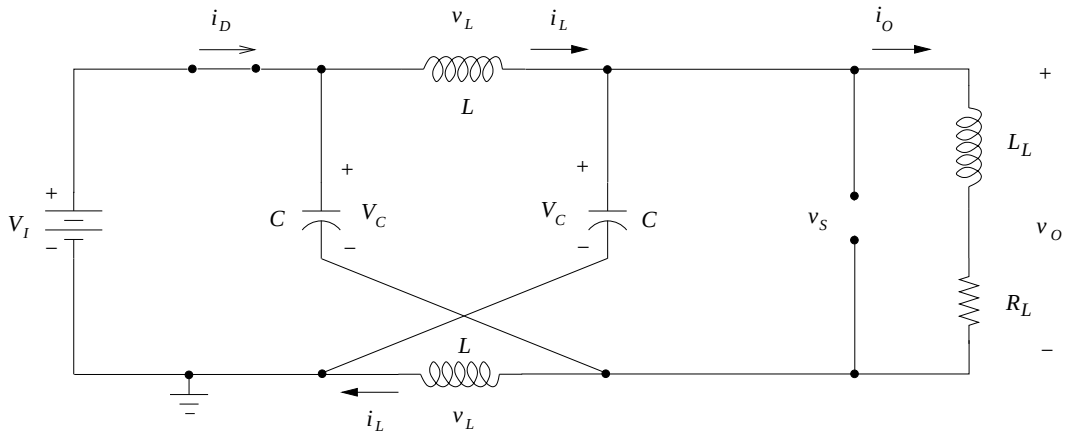

Figure 3.3: Equivalent circuit of the PWM Z-source converter when the switch is OFF and the diode is ON.

$$= \frac{V_I - V_C}{L} \int_{DT}^{t} dt + i_L(DT)$$
$$= \frac{V_I - V_C}{L}(t - DT) + i_L(DT) \tag{3.11}$$

where $i_L(DT)$ is the initial condition of the inductor current. The peak-to-peak ripple of the inductor current is

$$\Delta i_L = i_L(DT) - i_L(T)$$
$$= i_L(DT) - \frac{(V_I - V_C)}{L} T(1 - D) - i_L(DT)$$
$$= -\frac{(V_I - V_C)}{f_S L}(1 - D) \tag{3.12}$$

The voltage across the diode and the current through the switch is zero. The idealized waveforms associated with the Z-source converter operating in CCM is shown in Fig. 3.4.

3.4.3 DC Voltage Transfer Function for CCM

Based on Faraday's law of electromagnetic induction the voltage across an inductor as a function of time is

$$v_L = L \frac{di_L}{dt} \tag{3.13}$$

or

$$\frac{1}{L} v_L dt = di_L. \tag{3.14}$$

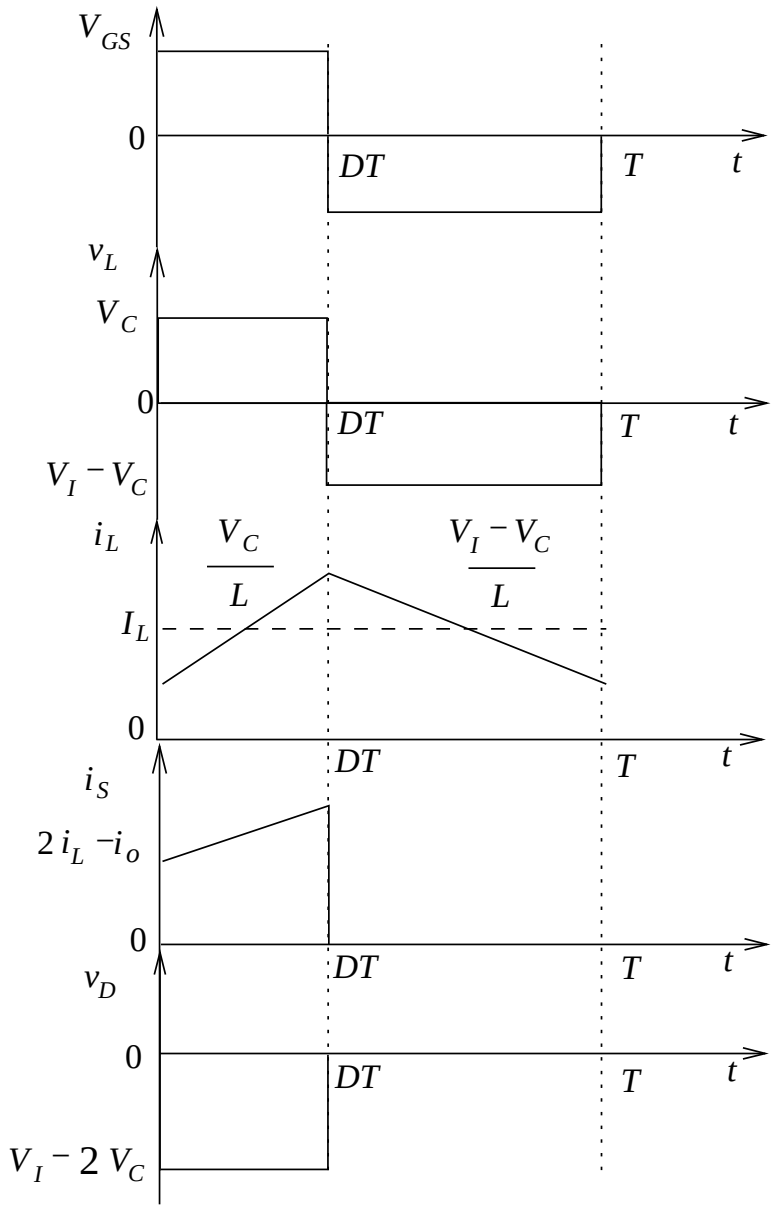

Figure 3.4: Idealized steady state waveforms of PWM Z-source converter operating in CCM.

Integrating (3.14) over one switching time period T

$$\int_0^T \frac{1}{L} v_L dt = \int_0^T di_L \tag{3.15}$$

or

$$\frac{1}{L}\int_0^T v_L dt = i_L(T) - i_L(0) = 0 \tag{3.16}$$

or

$$\int_0^T v_L dt = 0. \tag{3.17}$$

Since, for steady state condition $i_L(T) = i_L(0)$. Equation (3.17) is popularly referred to as the *volt-second balance* for an inductor. By applying volt-second balance to the Z network inductor we can obtain the dc input to capacitor voltage transfer function [6], [31] - [33]. From (3.5), (3.10) and (3.17)

$$\int_0^{DT} v_L(t)dt + \int_{DT}^T v_L(t)dt = 0$$

$$V_C T(D) + (V_I - V_C)T(1-D) = 0$$

$$V_C(D' - D) = V_I D'$$

$$\frac{V_C}{V_I} = \frac{D'}{D' - D} = \frac{1-D}{1-2D} \tag{3.18}$$

where $D' = 1 - D$. Equation (3.18) is the dc voltage transfer function of PWM Z-source dc-dc converter [6], [31] - [33]. From Fig. 3.5 it can be seen that M_{VDC} asymptotically reaches infinity as D tends to 0.5. Since V_C is the dc voltage across the load, the dc output voltage V_O is the same as V_C. This condition is not applicable for ac large or small signals. Based on the principle of conservation of energy $V_I I_I$=$V_O I_O$, and (3.18) we can obtain the dc current transfer function as

$$M_{IDC} = \frac{I_I}{I_O} = \frac{D'}{D' - D} = \frac{1-D}{1-2D}. \tag{3.19}$$

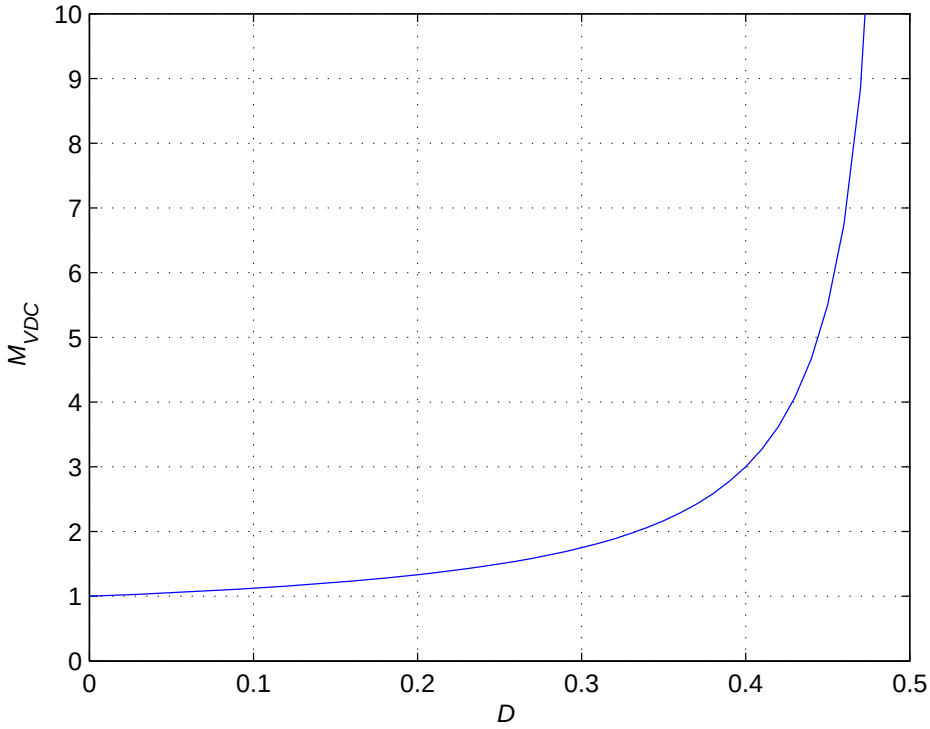

Figure 3.5: DC voltage transfer function M_{VDC} as a function of duty ratio D for an ideal PWM Z-source converter in CCM.

3.5 Verification by Simulation

Consider an open-loop PWM Z-source converter with the following specifications: $V_I = 12$ V, $f_s = 40$ kHz, $R_O = 50\ \Omega$, $L_O = 330\ \mu$H, $C_1 = C_2 = 220\ \mu$ F, and $L_1 = L_2 = 330\ \mu$ H. Choosing the duty ratio D to be 0.3, based on (3.18)

$$\frac{V_C}{V_I} = \frac{D'}{D' - D} = \frac{1 - D}{1 - 2D}$$

$$V_C = V_I \frac{1 - D}{1 - 2D} = \frac{1 - 0.3}{1 - 0.6}$$

$$V_C = 1.75 V_I = 21 \text{ V}. \tag{3.20}$$

During the time interval $0 \leq t \leq DT$ the voltage across the diode is

$$v_D = V_I - 2V_C = -30 \text{ V}, \tag{3.21}$$

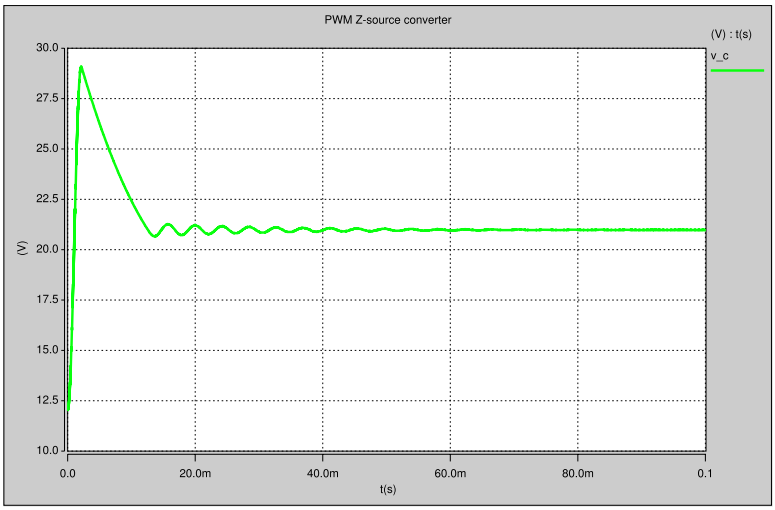

Figure 3.6: V_C as a function of t for $D = 0.3$ and $V_I = 12$ V obtained by Saber.

and the voltage across the Z inductor L is

$$v_L = V_C = 21 \text{ V}. \tag{3.22}$$

During the interval $DT \leq t \leq T$, the current through and the voltage across S and D are zero respectively. This is true for ideal semiconductor devices only. The voltage across the Z inductor is

$$v_L = V_I - V_C = -9 \text{ V}. \tag{3.23}$$

circuit simulator. Ideal semiconductor switches and passive components were employed. Capacitor voltage V_C as a function of time for $D = 0.3$ is shown in Fig. 3.6. The key voltages and currents for one time period is shown in Fig. 3.7. The values expected by (3.21) - (3.23) are in excellent agreement with the corresponding values shown in Fig. 3.7. Equation (3.9) is validated in Fig. 3.8.

3.6 Small-Signal Modeling of the PWM Z-Source Converter

Fig. 3.10 shows the power stage of the PWM Z-source converter. v_i represents the small-signal perturbation in the input voltage, and d represents the small-signal variation in the control parameter or the duty cycle. The dominant non-linearity

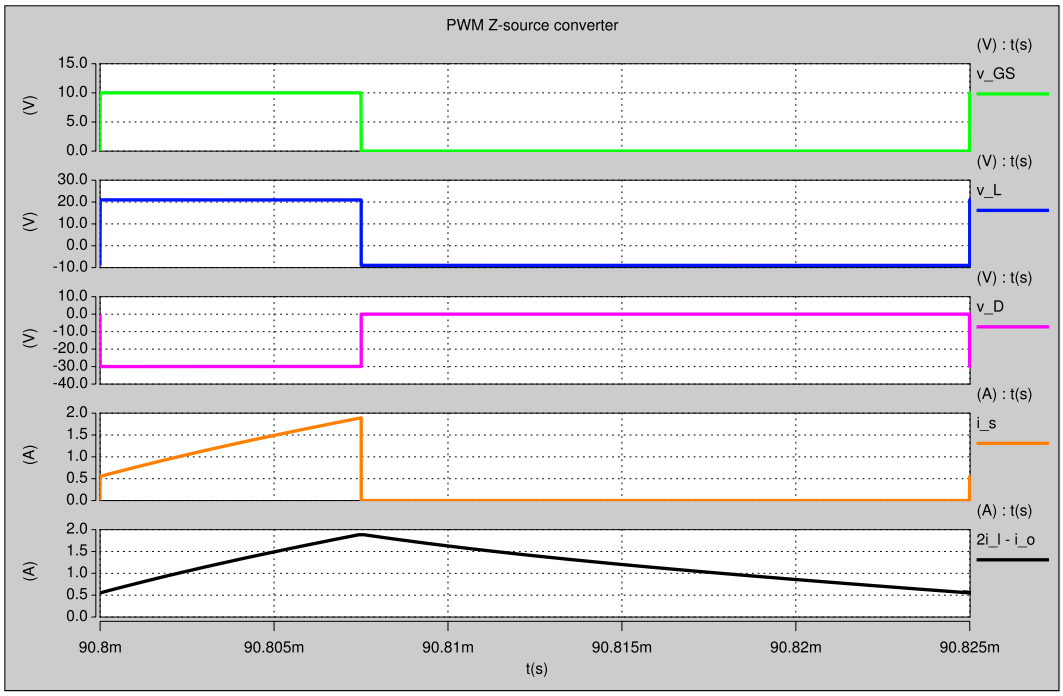

Figure 3.7: Saber simulation waveforms of v_{GS}, v_L, i_L, v_D, and i_S as a function of time t.

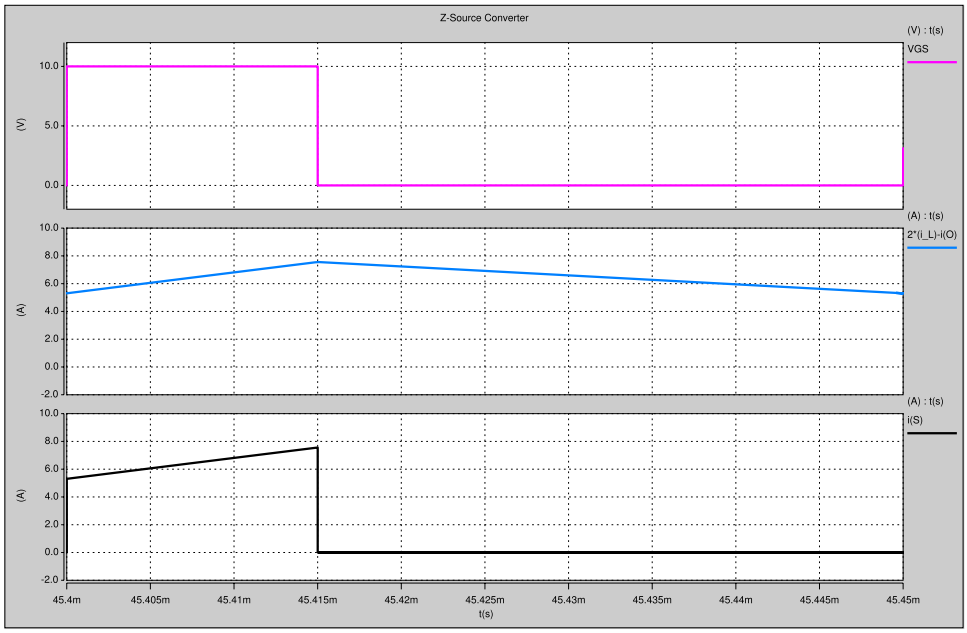

Figure 3.8: Saber simulation waveforms of v_{GS}, $2i_L - i_O$, and i_S as functions of time t.

in the PWM Z-source converter is due to the effect of the semiconductor switches MOSFET S and the diode D being operated as switches. The passive components

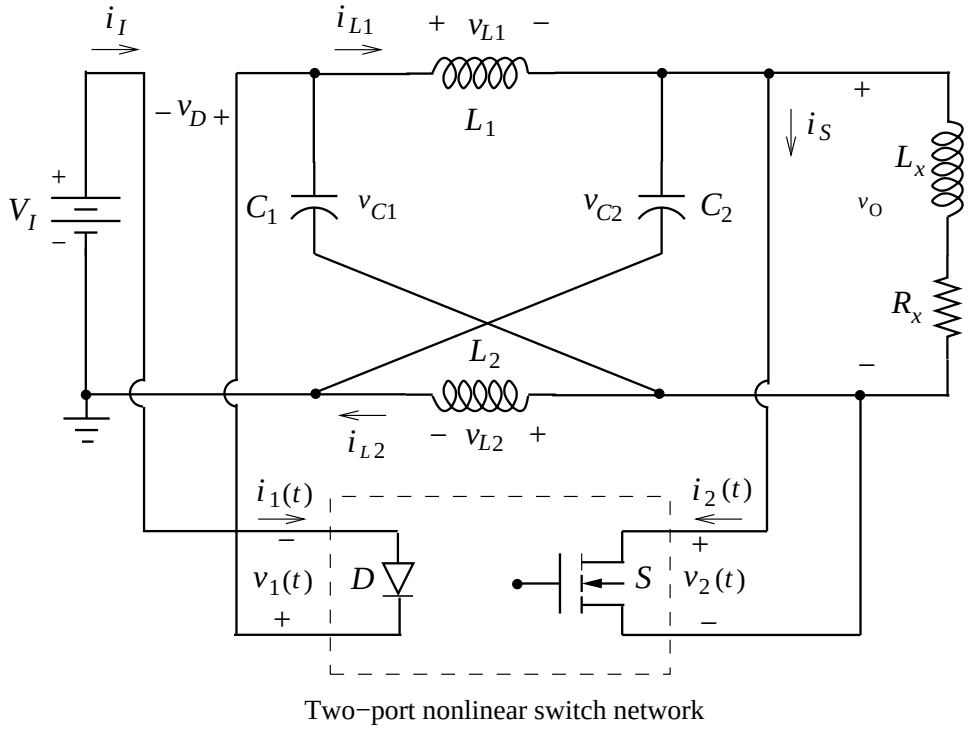

Figure 3.9: PWM Z-source converter with the nonlinear switch circuit.

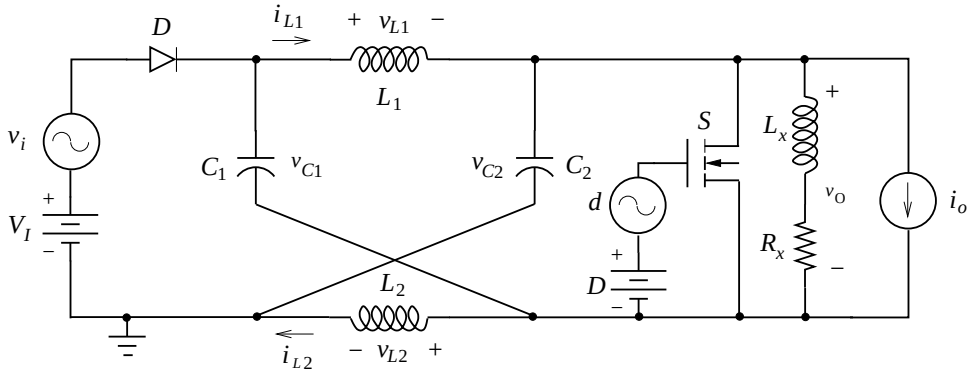

Figure 3.10: PWM Z-source converter with small-signal variations v_i, d, and i_o.

such as the inductors, capacitors, and the resistors are linear and time-invariant. The task of linearizing the PWM Z-source converter is to essentially replace the semiconductor switch network by an appropriate linear model [21]. Some portions of this section are published in [21]. The following assumptions are valid through the entire analysis:

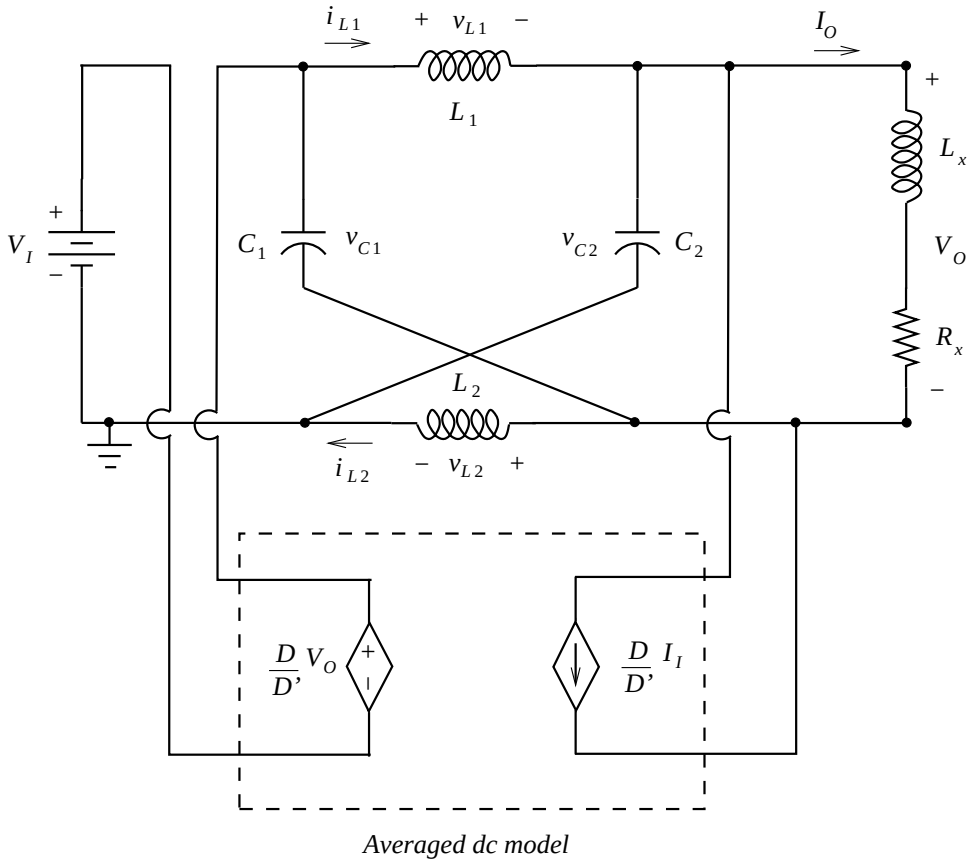

Figure 3.11: Averaged dc model of the PWM Z-source converter operating in CCM.

1. Inductors, capacitors, and resistors are linear, time-invariant, and frequency independent. (However, it should be noted that the parasitic resistances of the inductors and the capacitors can be considered once the transfer functions are obtained in the impedance form)

2. Semiconductor switches, i.e., the MOSFET and the diode are ideal.

3. The natural time constant of the converter is much larger than one switching time period.

The Z impedance network is symmetric, that is $C_1 = C_2 = C$ and $L_1 = L_2 = L$. As a consequence of the symmetry, we get $v_{C1} = v_{C2} = v_C$ and $i_{L1} = i_{L2} = i_L$. From basic steady-state circuit analysis, the averaged dc values of the current through the

MOSFET S and the voltage across the diode D are

$$I_S = \frac{D}{D'} I_I \tag{3.24}$$

and

$$V_D = \frac{D}{D'} V_O, \tag{3.25}$$

where D is the steady-state duty ratio of the switch S and $D' = 1 - D$. Equations (3.24) and (3.25) represent the averaged dc model of the PWM Z-source converter operating in CCM. Fig. 3.11 shows the averaged dc model of the PWM Z-source converter operating in CCM. The steady-state dc input-to-capacitor voltage conversion ratio obtained by applying volt-second balance to the Z-network inductor is [33]

$$M_{VDC} = \frac{V_C}{V_I} = \frac{1 - D}{1 - 2D}. \tag{3.26}$$

By replacing the averaged dc quantities by low frequency, large-signal time-dependent quantities, we obtain the large-signal averaged averaged model of the PWM Z-source converter. The averaged dc components I_S, I_I, V_D, V_O, and D are replaced by i_S, i_I, v_D, v_O, and d_T. The relationships among the large-signal quantities can be approximated by the relationships existing amongst the dc quantities as

$$i_S \approx \frac{d_T}{d_T{}'} i_I \tag{3.27}$$

and

$$v_D \approx \frac{d_T}{d_T{}'} v_O. \tag{3.28}$$

Equations (3.27) and (3.28) represent the low-frequency large-signal model of the semiconductor switch network of the PWM Z-source converter operating in CCM. Fig. 3.12 shows the averaged dc model of the PWM Z-source converter operating in CCM. In (3.27) and (3.28), we have duty ratio $d_T = D + d$, switch current $i_S = I_S + i_s$, voltage across the diode $v_D = V_D + v_d$, input current $i_I = I_I + i_i$, and output voltage

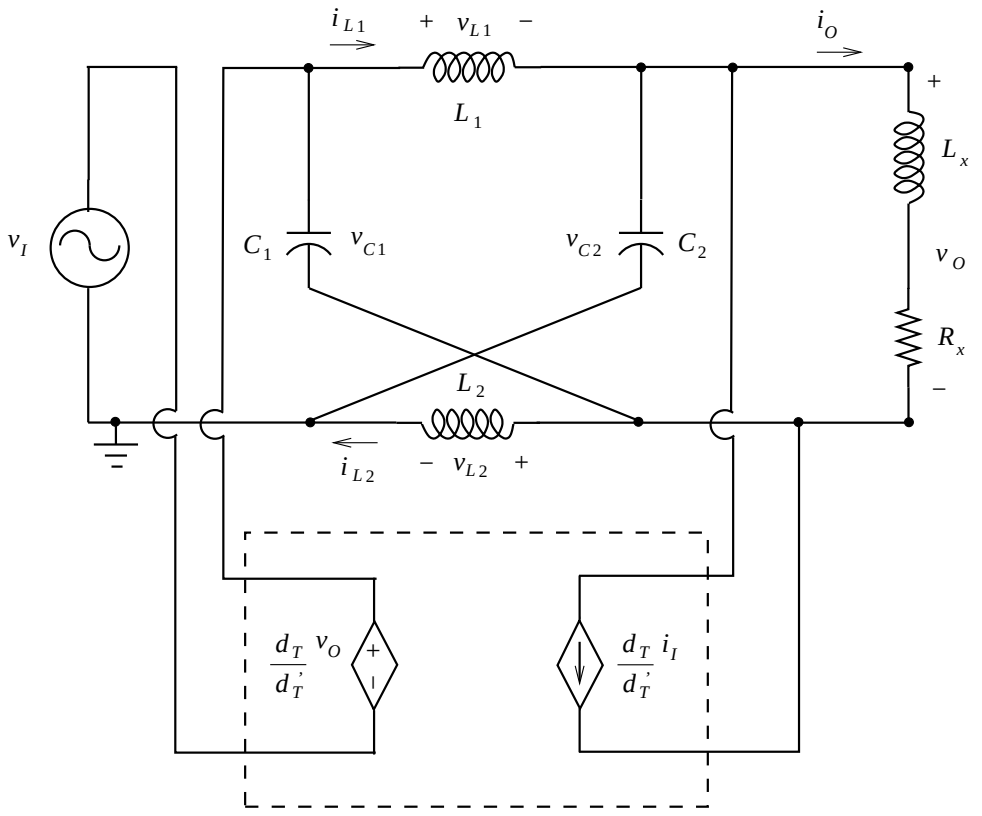

Figure 3.12: Low-frequency large-signal model of the PWM Z-source converter operating in CCM.

$v_O = V_O + v_o$. Quantities D, I_S, I_I, V_D, and V_O are dc components, and d, i_s, i_i, v_d, and v_o are ac components. Consequently, (3.27) and (3.28) can be written as

$$i_S = I_S + i_s = \frac{D+d}{D'-d}(I_I + i_i)$$
$$= \frac{D+d}{D'}\frac{1}{(1-\frac{d}{D'})}(I_I + i_i), \tag{3.29}$$

and

$$v_D = V_D + v_d = \frac{D+d}{D'-d}(V_O + v_o)$$
$$= \frac{D+d}{D'}\frac{1}{(1-\frac{d}{D'})}(V_O + v_o). \tag{3.30}$$

Maclaurin series expansion of $\frac{1}{1-\frac{d}{D'}}$ for $-1 < \frac{d}{D'} > 1$ is given by

$$\frac{1}{1-\frac{d}{D'}} = 1 + \frac{d}{D'} + (\frac{d}{D'})^2 + ... + (\frac{d}{D'})^n \tag{3.31}$$

Since, by definition d is small-signal perturbation $d << D$ or $\frac{d}{D'} << 1$. For $|\frac{d}{D'}| << 1$, 1^{st} order approximation of the Maclaurin series reduces (3.31) to

$$\frac{1}{1-\frac{d}{D'}} = 1 + \frac{d}{D'}. \tag{3.32}$$

Substituting (3.32) into (3.29) and (3.30) yields

$$i_S = I_S + i_s = \frac{D+d}{D'}\left(1+\frac{d}{D'}\right)(I_I + i_i) \tag{3.33}$$

and

$$v_D = V_D + v_d = \frac{D+d}{D'}\left(1+\frac{d}{D'}\right)(V_O + v_o). \tag{3.34}$$

Expanding (3.33) and (3.34), and noting that $D + D' = 1$, we get

$$i_S = \frac{D}{D'}I_I + \frac{D}{D'}i_i + \frac{I_I}{D'^2}d + \frac{I_I}{D'^2}d^2 + \frac{di_i}{D'^2} + \frac{d^2 i_i}{D'^2} \tag{3.35}$$

and

$$v_D = \frac{D}{D'}V_O + \frac{D}{D'}v_o + \frac{V_O}{D'^2}d + \frac{V_O}{D'^2}d^2 + \frac{dv_o}{D'^2} + \frac{d^2 v_o}{D'^2}. \tag{3.36}$$

Equations (3.35) and (3.36) represent the bilinear model of the PWM Z-source converter operating in CCM [21]. Fig. 3.13 shows the bilinear dc model of the PWM Z-source converter operating in CCM. When the following small-signality conditions are satisfied $d << DD'$, $i_i << I_I$, and $v_o << V_O$, equations (3.35) and (3.36) reduce to

$$i_S = I_S + i_s = \frac{D}{D'}I_I + \frac{D}{D'}i_i + \frac{I_I}{D'^2}d \tag{3.37}$$

and

$$v_D = V_D + v_d = \frac{D}{D'}V_O + \frac{D}{D'}v_o + \frac{V_O}{D'^2}d. \tag{3.38}$$

Alternatively, ignoring the products of two small-signal terms and higher order (> 1) small-signal terms, (3.35) and (3.36) reduce to (3.37) and (3.38). Equations (3.37) and (3.38) are linearized due to the small-signality conditions, and they represent the dc and linear small-signal model of semiconductor switch network of the PWM Z-source converter operating in CCM [21]. Equations (3.37) and (3.38) can be realized

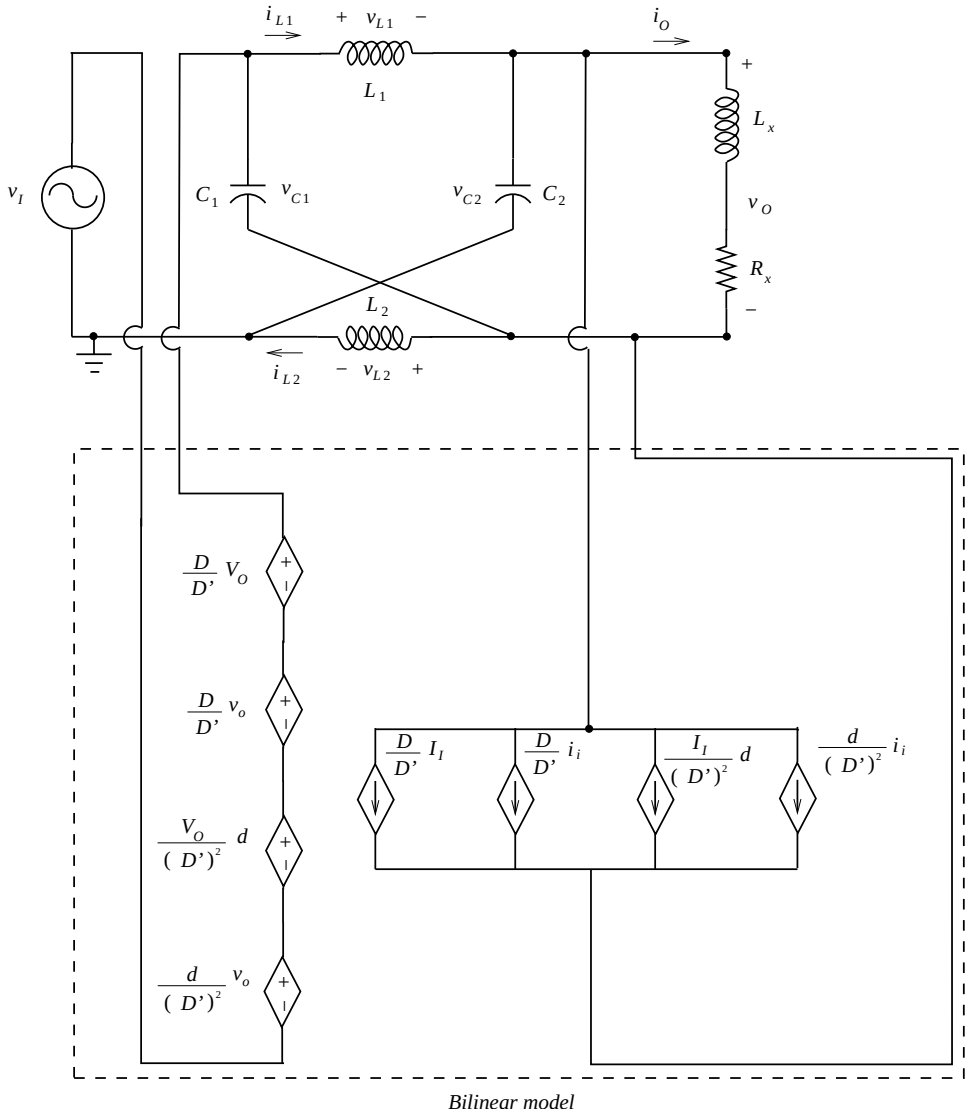

Figure 3.13: Bilinear model of the PWM Z-source converter operating in CCM.

by using voltage-controlled voltage sources and current-controlled current-sources to obtain an equivalent dc and small-signal circuit model of the PWM Z-source converter in CCM as shown in Fig. 3.14 [21]. Since (3.37) and (3.38) are linearized, the dc and the small-signal components can be segregated to get the dc and the small-signal models respectively. The dc model of the PWM Z-source converter is described by

$$I_S = \frac{D}{D'} I_I \tag{3.39}$$

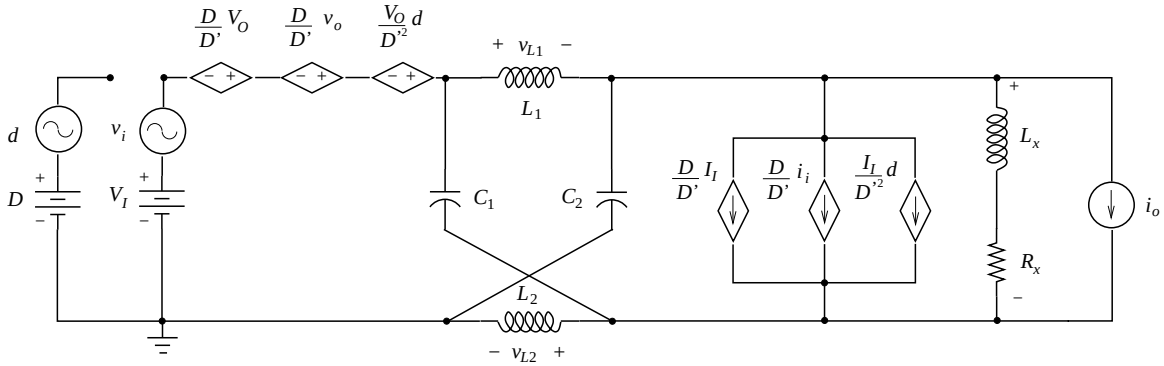

Figure 3.14: DC and small-signal model of the PWM Z-source converter operating in CCM.

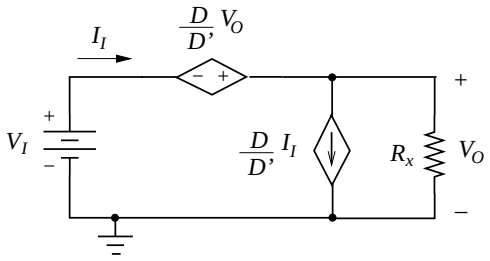

Figure 3.15: DC model of the PWM Z-source converter operating in CCM.

and

$$V_D = \frac{D}{D'}V_O. \tag{3.40}$$

Equations (3.39) and (3.40) can be realized by using a voltage-controlled voltage source and a current-controlled current-source to obtain an equivalent dc circuit model of the PWM Z-source converter in CCM as shown in Fig. 3.15. The ac small-signal linear model of the PWM Z-source converter is described by

$$i_s = \frac{D}{D'}i_i + \frac{I_I}{D'^2}d \tag{3.41}$$

and

$$v_d = \frac{D}{D'}v_o + \frac{V_O}{D'^2}d. \tag{3.42}$$

Equations (3.41) can (3.42) be realized by using voltage-controlled voltage sources and current-controlled current-sources to obtain an equivalent ac small-signal circuit model of the PWM Z-source converter in CCM as shown in Fig. 3.16. The small-

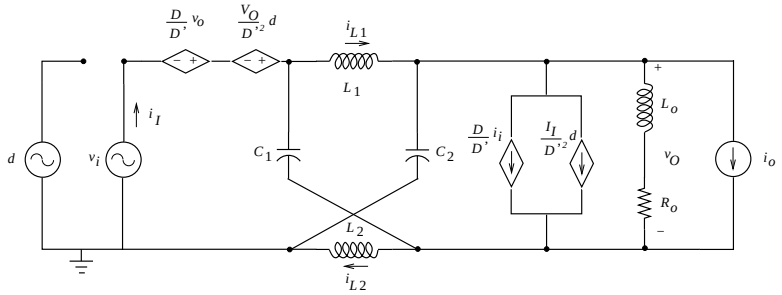

Figure 3.16: Small-signal model of the PWM Z-source converter operating in CCM.

signal model derived is valid from dc to half the switching frequency.

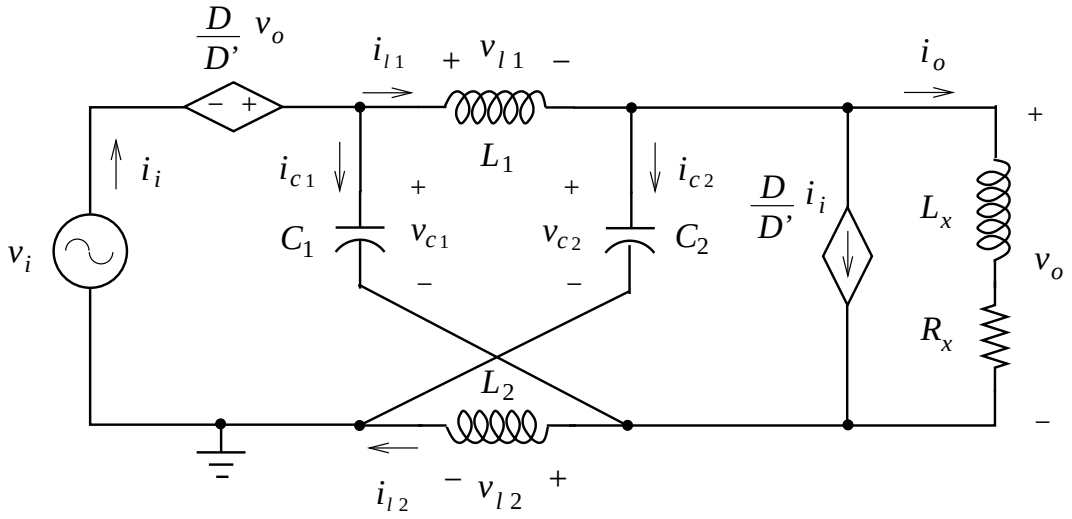

Figure 4.1: Small-signal model of PWM Z-source converter to derive the open-loop input voltage-to-capacitor voltage and input voltage-to-inductor current transfer functions.

4 Open-Loop Power-Stage Transfer Functions of PWM Z-Source Converter for CCM

4.1 Open-Loop Input Voltage-to-Capacitor Voltage Transfer Function

By letting $d = 0$ and $i_o = 0$ in Fig. 3.16, we obtain the small-signal model of the PWM Z-source converter for determining the open-loop input voltage-to-capacitor voltage transfer function. The small-signal model for deriving the open-loop input voltage-to-capacitor voltage transfer function is shown in Fig. 4.1 [21]. Since $L_1 = L_2 = L$, and $C_1 = C_2 = C$, and due to the symmetry of the Z network $i_{l1} = i_{l2} = i_l$ and $v_{c1} = v_{c2} = v_c$. By Kirchoff's current law, we get

$$i_i = i_l + i_c, \tag{4.1}$$

and

$$i_l = i_c + \frac{D}{D'} i_i + i_o. \tag{4.2}$$

By Kirchoff's voltage law, we get

$$v_i + \frac{D}{D'} v_o - i_l Z_L - v_c = 0, \tag{4.3}$$

and

$$v_c - v_o - i_l Z_L = 0. \tag{4.4}$$

By substituting i_i from (4.1) in (4.2) we obtain i_l in terms of i_c and i_o as shown below,

$$i_l = i_c + \frac{D}{D'}(i_l + i_c) + i_o$$

$$i_l - \frac{D}{D'} i_l = i_c + \frac{D}{D'} i_c + i_o$$

$$i_l(1 - \frac{D}{D'}) = i_c(1 + \frac{D}{D'}) + i_o$$

$$i_l \frac{D' - D}{D'} = i_c \frac{1}{D'} + i_o$$

$$i_l = (\frac{D'}{D' - D})(\frac{i_c}{D'} + i_o) \tag{4.5}$$

By substituting for i_l from (4.5) in (4.4) and noting that $i_c = v_c/Z_C$ and $i_o = v_o/Z_x$, we get

$$v_c - v_o - Z_L(\frac{1}{D' - D} i_c + \frac{D'}{D' - D} i_o) = 0$$

$$v_c(1 - \frac{1}{D' - D}\frac{Z_L}{Z_C}) = v_o(1 + \frac{D'}{D' - D}\frac{Z_L}{Z_x}) \tag{4.6}$$

or

$$v_o = v_c \left[\frac{1 - \frac{Z_L}{(D'-D)Z_C}}{1 + \frac{D'Z_L}{(D'-D)Z_x}} \right]. \tag{4.7}$$

On simplification (4.7) becomes

$$v_o = v_c \frac{Z_x}{Z_C} \left[\frac{(D' - D)Z_C - Z_L}{(D' - D)Z_x + D'Z_L} \right]. \tag{4.8}$$

By substituting (4.8) in (4.5) to get i_l in terms of v_c, we get

$$i_l = \frac{1}{D' - D}\frac{v_c}{Z_C} + \frac{D'}{D' - D}\frac{v_c}{Z_x}\frac{Z_x}{Z_C} \left[\frac{(D' - D)Z_C - Z_L}{(D' - D)Z_x + D'Z_L} \right]$$

$$= \frac{1}{D' - D}\frac{v_c}{Z_C} \left[1 + D' \left(\frac{(D' - D)Z_C - Z_L}{(D' - D)Z_x + D'Z_L} \right) \right]$$

$$= \frac{1}{D'-D}\frac{v_c}{Z_C}\left[\frac{(D'-D)Z_x + D'Z_L + D'(D'-D)Z_C - D'Z_L}{(D'-D)Z_x + D'Z_L}\right]$$

$$i_l = \frac{v_c}{Z_C}\left[\frac{Z_x + D'Z_C}{(D'-D)Z_x + D'Z_L}\right]. \tag{4.9}$$

Substituting (4.8) and (4.9) in (4.3), we get

$$v_i = v_c + v_c\frac{Z_L}{Z_C}\left[\frac{Z_x + D'Z_C}{(D'-D)Z_x + D'Z_L}\right] - v_c\frac{D}{D'}\frac{Z_x}{Z_C}\left[\frac{(D'-D)Z_C - Z_L}{(D'-D)Z_x + D'Z_L}\right]$$

$$\frac{v_i}{v_c} = 1 + \frac{Z_L}{Z_C}\left[\frac{Z_x + D'Z_C}{(D'-D)Z_x + D'Z_L}\right] - \frac{D}{D'}\frac{Z_x}{Z_C}\left[\frac{(D'-D)Z_C - Z_L}{(D'-D)Z_x + D'Z_L}\right]$$

$$= \frac{Z_C[(D'-D)Z_x + D'Z_L]D' + D'Z_L(Z_x + D'Z_C) - DZ_x[(D'-D)Z_C - Z_L]}{D'Z_C[(D'-D)Z_x + D'Z_L]}$$

$$= \frac{D'Z_C(D'-D)Z_x + D'^2Z_CZ_L + D'Z_LZ_x + D'^2Z_LZ_C - D(D'-D)Z_xZ_C + DZ_xZ_L}{D'(D'-D)Z_CZ_x + D'^2Z_CZ_L}$$

$$= \frac{(D'-D)^2Z_xZ_C + 2D'^2Z_LZ_C + (D'+D)Z_LZ_x}{D'(D'-D)Z_CZ_x + D'^2Z_CZ_L}$$

$$\frac{v_i}{v_c} = \frac{(D'-D)^2Z_xZ_C + 2D'^2Z_LZ_C + Z_LZ_x}{D'^2Z_CZ_x - DD'Z_CZ_x + D'^2Z_CZ_L}$$

$$\frac{v_c}{v_i} = \frac{D'^2Z_CZ_x - DD'Z_CZ_x + D'^2Z_CZ_L}{(D'-D)^2Z_xZ_C + 2D'^2Z_LZ_C + Z_LZ_x}. \tag{4.10}$$

The s domain equivalent of the impedances are

$$Z_C = \frac{1}{sC}, \tag{4.11}$$

$$Z_x = R_x + sL_x, \tag{4.12}$$

and

$$Z_L = sL. \tag{4.13}$$

By substituting (4.11), (4.12), and (4.13) in (4.10), we get [21]

$$M_v(s) = \frac{v_c(s)}{v_i(s)} = \frac{D'^2\frac{1}{sC}(R_x + sL_x) - DD'\frac{1}{sC}(R_x + sL_x) + D'^2\frac{L}{C}}{\frac{1}{sC}(D' - D)^2(R_x + sL_x) + 2D'^2\frac{L}{C} + (R_x + sL_x)sL}$$

$$= \frac{D'^2R_x + D'^2L_xs - DD'R_x - DD'L_xs + D'^2Ls}{(D' - D)^2(R_x + sL_x) + 2D'^2Ls + (R_x + sL_x)LCs^2}$$

$$= \frac{(D'^2L_x - DD'L_x + D'^2L)s + D'^2R_x - DD'R_x}{(D' - D)^2R_x + (D' - D)^2L_xs + 2D'^2Ls + R_xLCs^2 + L_xLCs^3}$$

$$M_v(s) = \frac{[D'(D' - D)L_x + D'^2L]s + D'(D' - D)R_x}{L_xLCs^3 + R_xLCs^2 + [2D'^2L + (D' - D)^2L_x]s + (D' - D)^2R_x}. \tag{4.14}$$

4.1.1 Simulation and Experimental Results

Consider an example of the open-loop PWM Z-source converter with the following parameters: $f_s = 40$ kHz, $V_I = 12$ V, $D = 0.3$, $R_x = 50\ \Omega$, $L_x = 330\ \mu$H, $C_1 = C_2 = C = 220\ \mu$F, $L_1 = L_2 = L = 330\ \mu$H. Murata inductor 1433428C with measured ESR of 1.5 Ω at the switching frequency $f_s = 40$ kHz was used for L_1, L_2, and L_x. Electrolytic capacitors with measured capacitance of 220μ F and ESR of 0.2 Ω was used for C_1 and C_2. IRF530N Power MOSFET and U860 ultrafast recovery diode were employed as the switches. IR2110, a high side MOSFET driver was used to trigger the MOSFET. The experimental set up for obtaining M_v is based on [41] and as shown in Fig. 4.5. The parasitic resistances of the inductors and the capacitors are included in predicting the magnitude and phase of M_v by using (4.10). The impedances of the inductors and the capacitors are given by

$$Z_L = r_L + sL, \tag{4.15}$$

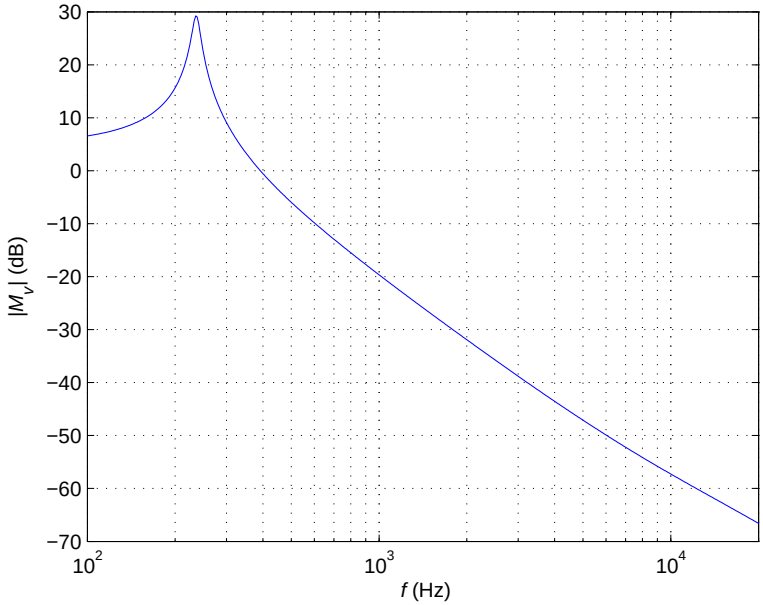

Figure 4.2: Theoretically predicted plot of $|M_v|$ for the lossless PWM Z-source converter operating in CCM.

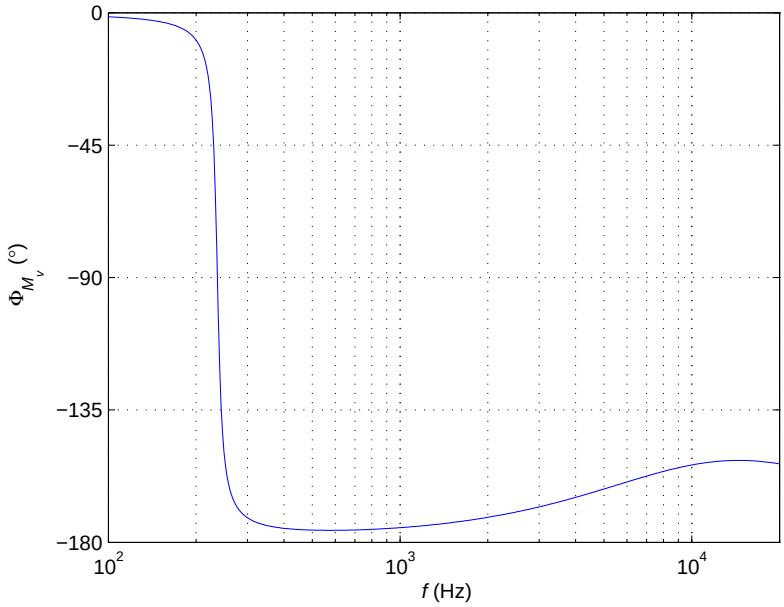

Figure 4.3: Theoretically predicted plot of ϕ_{M_v} for the lossless PWM Z-source converter operating in CCM.

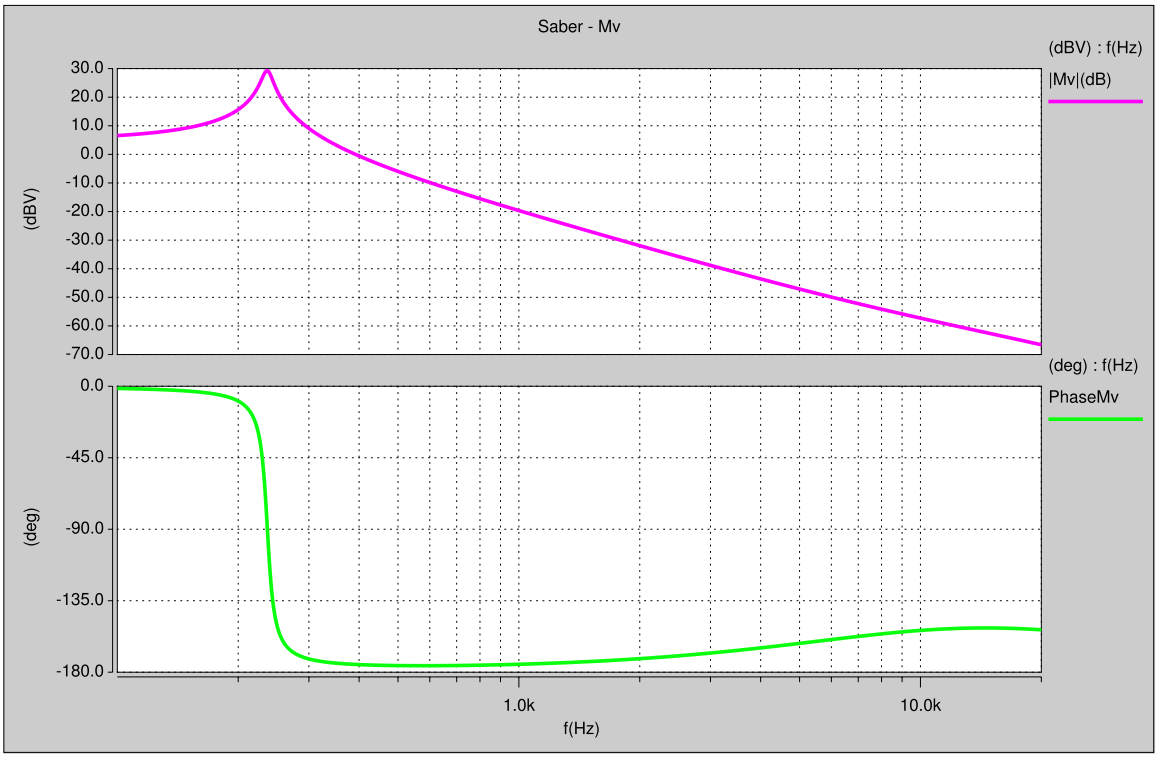

Figure 4.4: Simulated Bode plot of M_v for the lossless PWM Z-source converter operating in CCM.

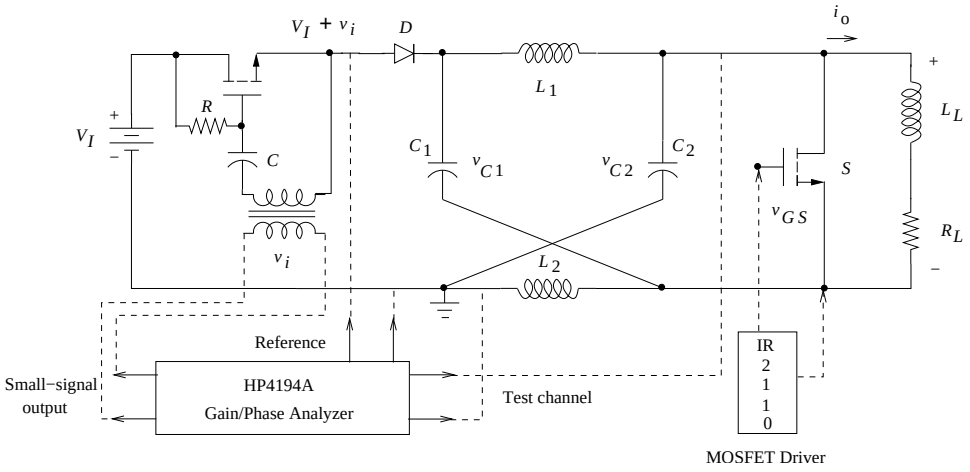

Figure 4.5: Schematic of experimental setup to measure M_v.

$$Z_C = r_C + \frac{1}{sC}, \tag{4.16}$$

and

$$Z_x = R_x + (sL_x + r_x). \tag{4.17}$$

The theoretically predicted Bode plots for $|M_v|$ and ϕ_{M_v} for a an ideal PWM Z-source converter (parasitics not included) are shown in Figs. 4.2 and 4.3, respectively. Fig. 4.4 shows the Bode plot obtained by simulating the small-signal model shown in Fig. 4.1 using Saber circuit simulator. Hewlett-Packard HP4194A Gain/Phase Analyzer was employed to obtain the Bode plots. SD250-1L gate drive transformer provided by Coilcraft was utilized as the gate-drive transformer corresponding to Fig. 4.5. The theoretically predicted and experimentally obtained Bode plots for $|M_v|$ and ϕ_{M_v} including the effect of parasitic resistances of the passive components are shown in Figs. 4.6 and 4.7, respectively. Fig. 4.8 shows the theoretically predicted response in v_C due to a step change in V_I from 0 to 5 V. Fig. 4.9 shows the experimentally obtained response in v_C due to a step change in V_I from 0 to 5 V.

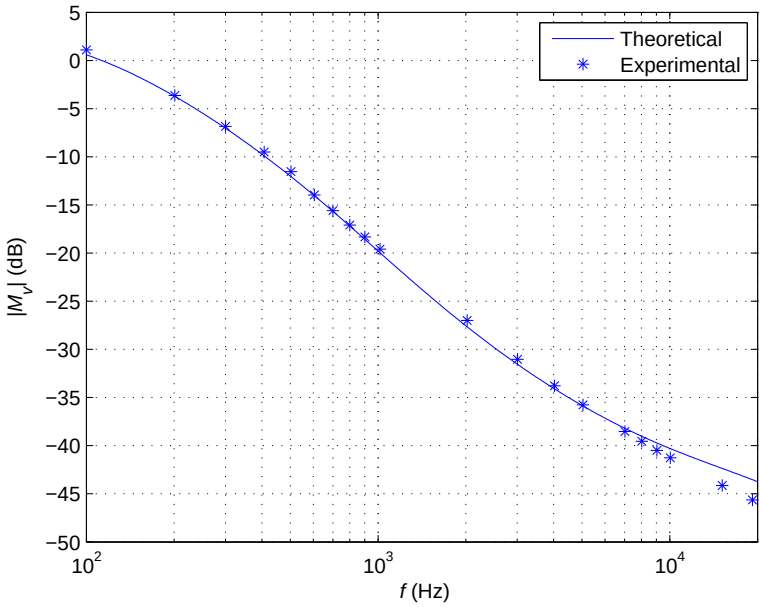

Figure 4.6: Theoretically predicted and experimentally obtained plot of $|M_v|$.

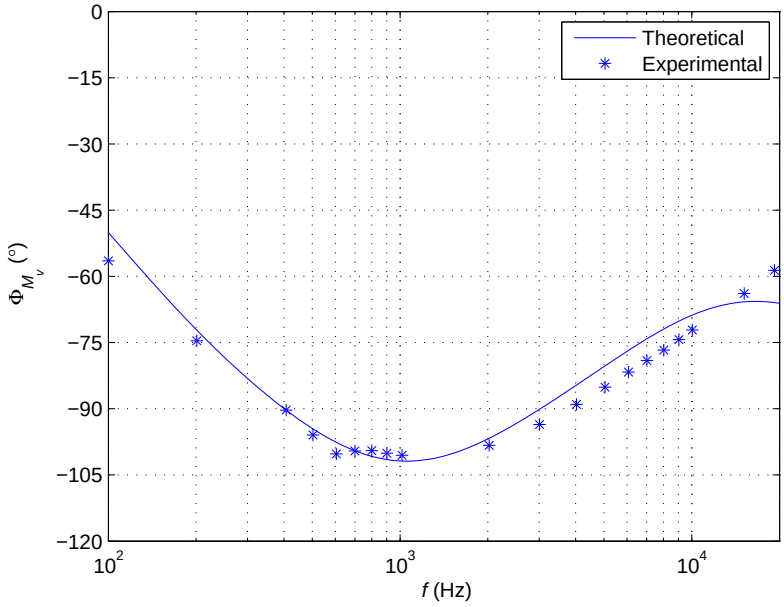

Figure 4.7: Theoretically predicted and experimentally obtained plot of ϕ_{M_v}.

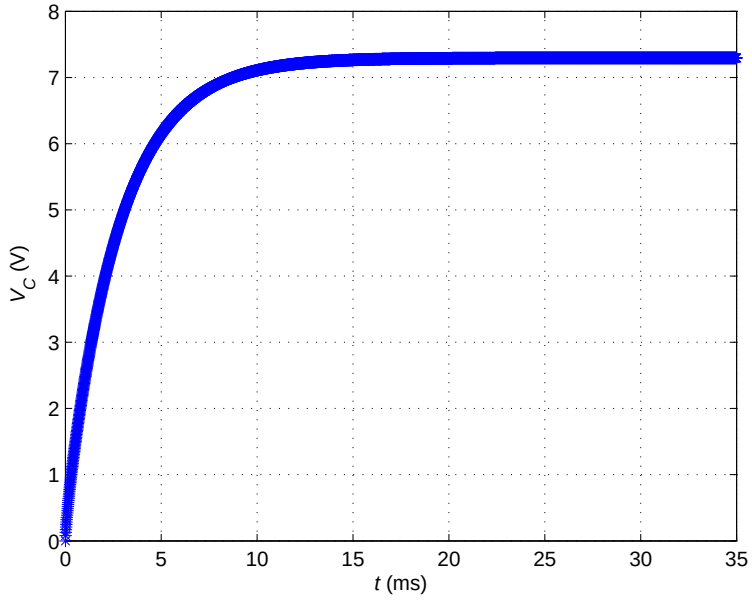

Figure 4.8: Theoretically predicted response in v_C due to a step change in V_I from 0 to 5 V.

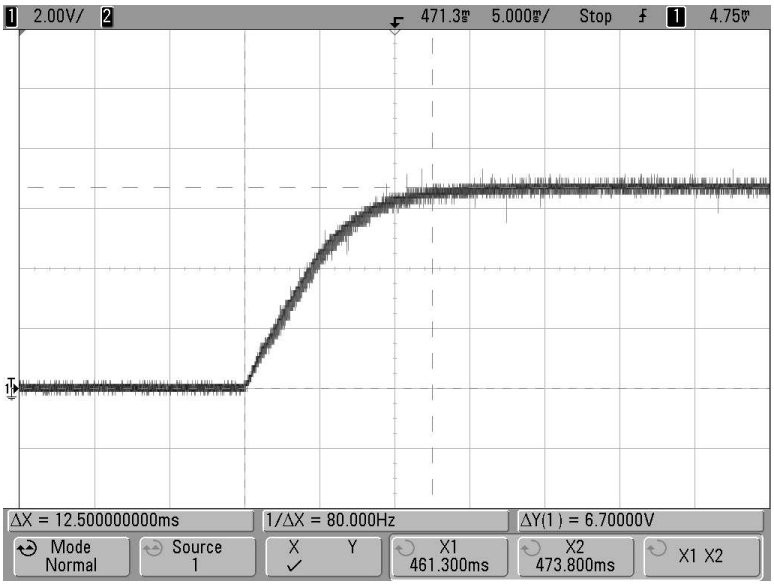

Figure 4.9: Experimentally obtained response in v_C due to a step change in V_I from 0 to 5 V.

4.2 Open-Loop Input Voltage-to-Inductor Current Transfer Function

The small-signal model obtained to derive the input-to-capacitor voltage transfer function can be employed to obtain the input-voltage-to-inductor-current transfer function M_{vi}. The small-signal model for deriving the open-loop input voltage-to-inductor current transfer function is shown in Fig. 4.1. By manipulating (4.9), we get

$$\frac{i_l}{v_c} = \frac{1}{Z_C}\left[\frac{Z_x + D'Z_C}{(D'-D)Z_x + D'Z_L}\right]. \tag{4.18}$$

Since $Z_C = 1/sC$, $Z_x = R_x + sL_x$, and $Z_L = sL$

$$\frac{i_l(s)}{v_c(s)} = \frac{L_xCs^2 + R_xCs + D'}{(D'-D)(R_x + sL_x) + D'sL}. \tag{4.19}$$

From (4.14) we have

$$\frac{v_c}{v_i}(s) = \frac{[D'(D'-D)L_x + D'^2L]s + D'(D'-D)R_x}{L_xLCs^3 + R_xLCs^2 + [2D'^2L + (D'-D)^2L_x]s + (D'-D)^2R_x}. \tag{4.20}$$

Using (4.19) and (4.20), we get

$$\frac{v_c}{v_i} \times \frac{i_l}{v_c} = \frac{i_l}{v_i}. \tag{4.21}$$

By substituting (4.19) and (4.20) in (4.21), we get

$$M_{vi} = \frac{i_l(s)}{v_i(s)} = \frac{D'L_xCs^2 + D'R_xCs + D'^2}{L_xLCs^3 + R_xLCs^2 + [2D'^2L + (D'-D)^2L_x]s + (D'-D)^2R_x}. \tag{4.22}$$

4.2.1 Simulation and Experimental Results

Consider an example of the open-loop PWM Z-source converter with the following parameters: $f_s = 40$ kHz, $V_I = 12$ V, $D = 0.3$, $R_x = 50\ \Omega$, $L_x = 330\ \mu$H, $C_1 = C_2 = C = 220\ \mu$F, $L_1 = L_2 = L = 330\ \mu$H. Murata inductor 1433428C with measured ESR of 1.5 Ω at the switching frequency $f_s = 40$ kHz was used for L_1, L_2, and L_x. Electrolytic capacitors with measured capacitance of 220μ F and ESR of 0.2 Ω was

used for C_1 and C_2. IRF530N Power MOSFET and U860 ultrafast recovery diode were employed as the switches. IR2110, a high side MOSFET driver was used to trigger the MOSFET. The experimental set up for obtaining M_{vi} is based on [41] and as shown in Fig. 4.5. The parasitic resistances of the inductors and the capacitors are included in predicting the magnitude and phase of M_v by using (4.10). The impedances of the inductors and the capacitors are given by

$$Z_L = r_L + sL, \tag{4.23}$$

$$Z_C = r_C + \frac{1}{sC}, \tag{4.24}$$

and

$$Z_x = R_x + (sL_x + r_x). \tag{4.25}$$

The theoretically predicted Bode plots for $|M_{vi}|$ and $\phi_{M_{vi}}$ for a an ideal PWM Z-source converter (parasitics not included) are shown in Figs. 4.10 and 4.11, respectively. Fig. 4.12 shows the Bode plot obtained by simulating the small-signal model shown in Fig. 4.1 using Saber circuit simulator. Hewlett-Packard HP4194A Gain/Phase Analyzer was employed to obtain the Bode plots. SD250-1L gate drive transformer provided by Coilcraft was utilized as the gate-drive transformer corresponding to Fig. 4.5. A Pearson Model 411 wide bandwidth ac current probe was employed to obtain the Bode plots for $|M_{vi}|$ and $\phi_{M_{vi}}$. The frequency response of the current probe was obtained for the same dc current level it would have during the experiment. The current probe frequency response was subtracted out using the compensation function while obtaining the Bode plots of M_{vi}. The theoretically predicted and experimentally obtained Bode plots for $|M_{vi}|$ and $\phi_{M_{vi}}$ including the effect of parasitic resistances of the passive components are shown in Figs. 4.14 and 4.15, respectively. Figs. 4.16 and 4.17 show the theoretically predicted and experimentally obtained responses in i_L due to a step change in V_I from 0 to 5 V. A 1 Ω sense resistor was added in series with the Z-network inductor L_2, and the voltage across it was

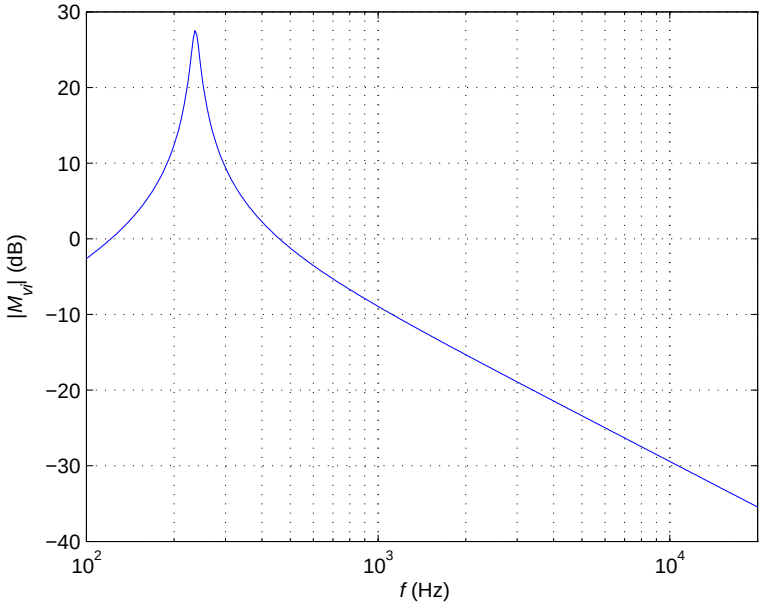

Figure 4.10: Theoretically predicted plot of $|M_{vi}|$ for the lossless PWM Z-source converter operating in CCM.

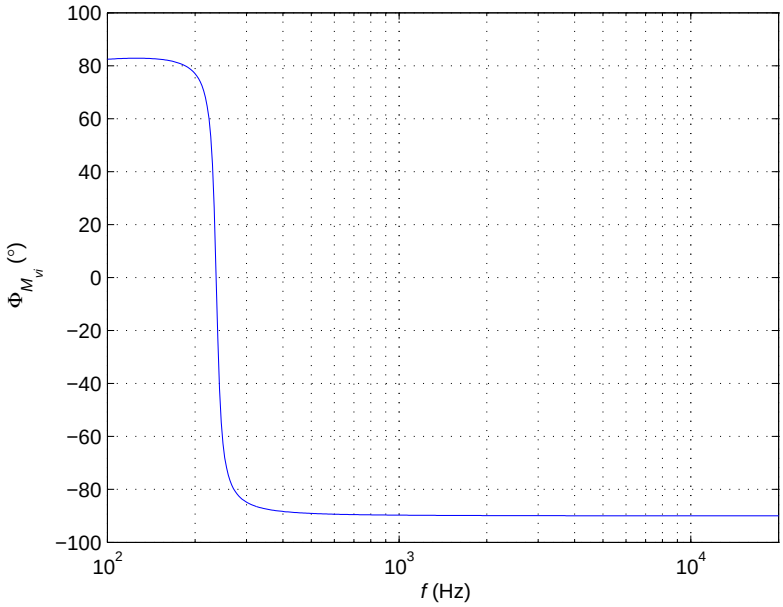

Figure 4.11: Theoretically predicted plot of $\phi_{M_{vi}}$ for the lossless PWM Z-source converter operating in CCM.

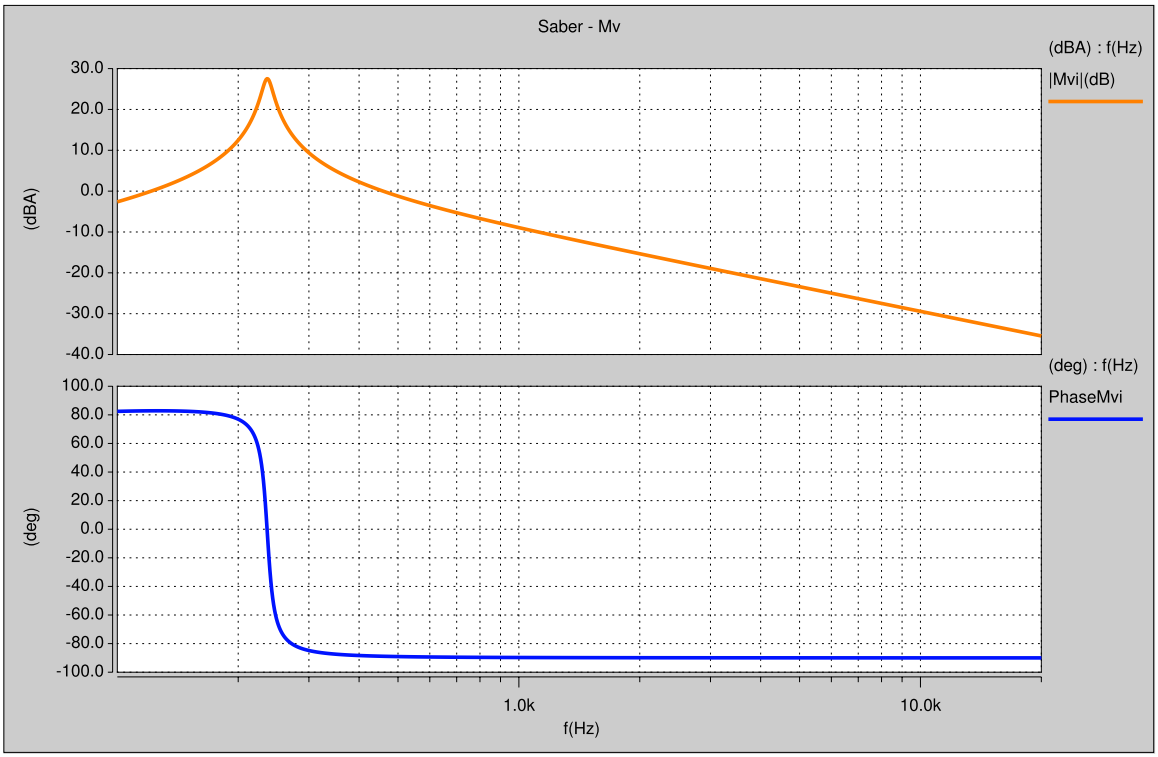

Figure 4.12: Simulated Bode plot of M_{vi} for the lossless PWM Z-source converter operating in CCM.

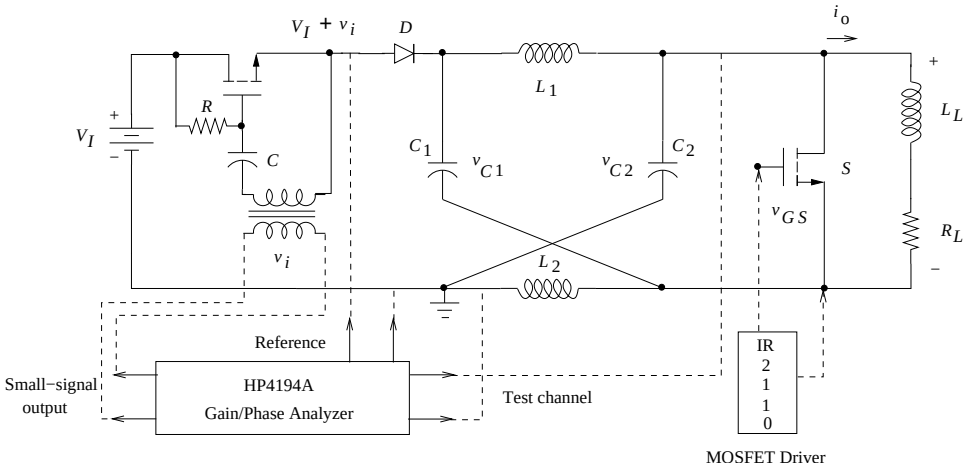

Figure 4.13: Schematic of experimental setup to measure M_{vi}.

recored to obtain the inductor current step response. The voltage-to-current scaling factor is 1 mA/mV The 1 Ω resistance was included in the ESR r_L of the Z-network inductor.

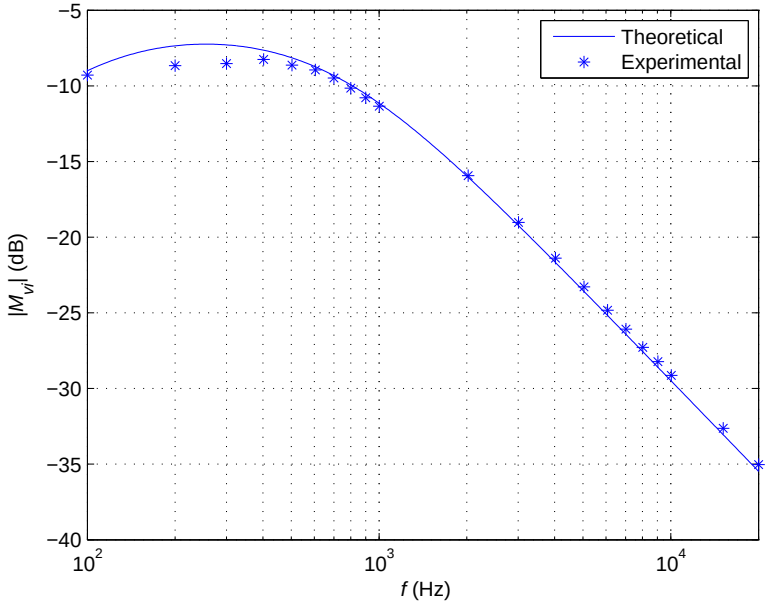

Figure 4.14: Theoretically predicted and experimentally obtained plot of $|M_{vi}|$.

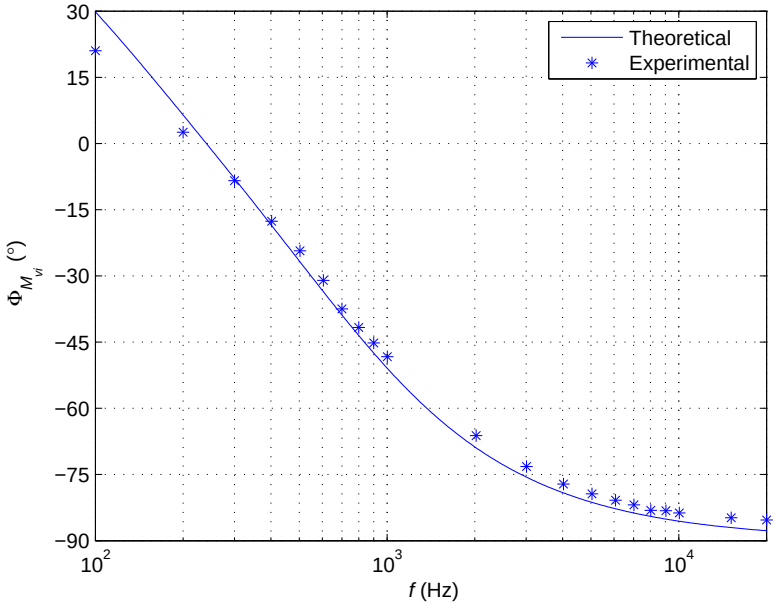

Figure 4.15: Theoretically predicted and experimentally obtained plot of $\phi_{M_{vi}}$.

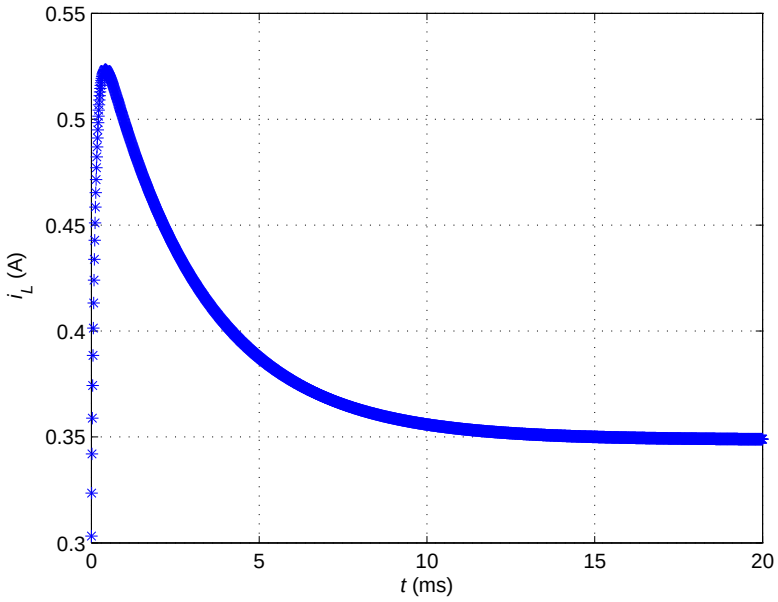

Figure 4.16: Theoretically predicted response in i_L due to a step change in V_I from 0 to 5 V.

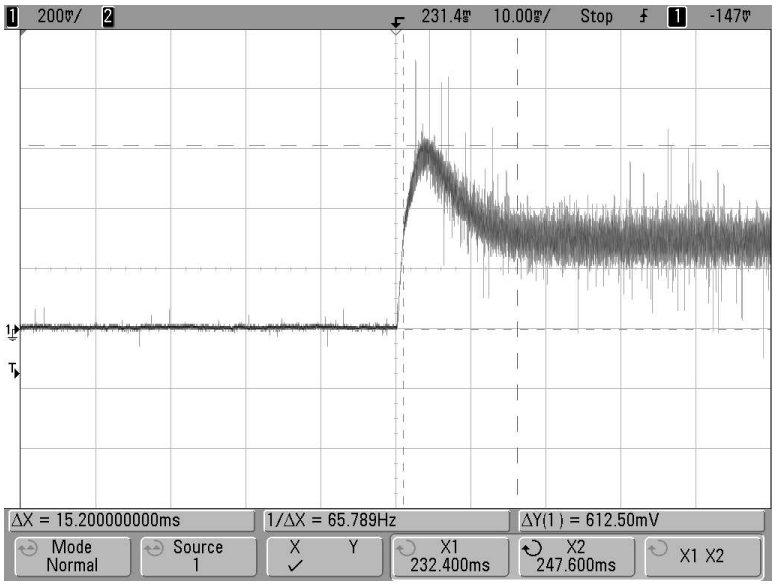

Figure 4.17: Experimentally obtained response in i_L due to a step change in V_I from 0 to 5 V.

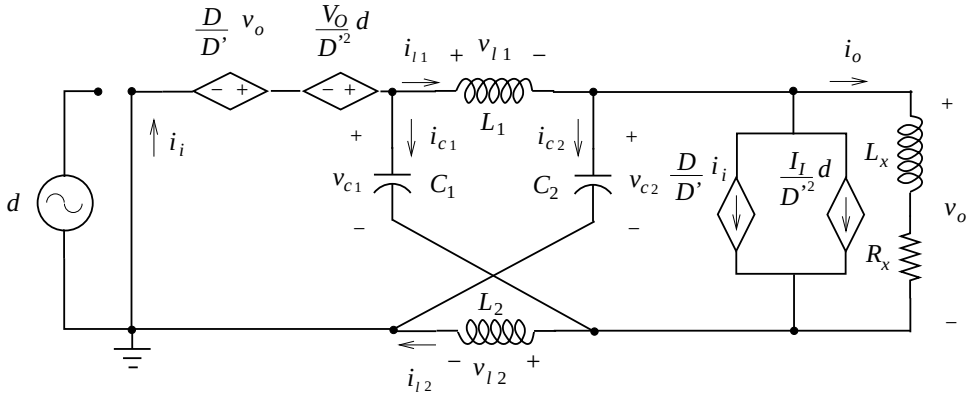

Figure 4.18: Small-signal to derive control-to-capacitor voltage transfer function for PWM Z-source converter in CCM.

4.3 Open-Loop Control-to-Capacitor Voltage Transfer Function

By setting $v_i = 0$ and $i_o = 0$ in 3.16, we obtain the small-signal model of the PWM Z-source converter for determining the open-loop input voltage-to-capacitor voltage transfer function as shown in Fig. 4.18. By Kirchoff's voltage law applied to the inner loop on the input side, inner loop on the load side, and the outer loop, we get

$$\frac{d}{D'^2}V_O + \frac{D}{D'}v_o - i_l Z_L - v_c = 0, \tag{4.26}$$

$$v_c - v_o - i_l Z_L = 0, \tag{4.27}$$

and

$$\frac{d}{D'^2}V_O + \frac{D}{D'}v_o - 2i_l Z_L - v_o = 0, \tag{4.28}$$

respectively. By Kirchoff's current law, we get

$$i_i = i_l + i_c, \tag{4.29}$$

and

$$i_l = i_c + \frac{D}{D'}i_i + \frac{d}{D'^2}I_I + i_o. \tag{4.30}$$

From (4.26) and (4.27), we get

$$i_l Z_L = \frac{d}{D'^2}V_O + \frac{D}{D'}v_o - v_c = 0 \tag{4.31}$$

and

$$i_l Z_L = v_c - v_o. \tag{4.32}$$

By equating the RHS of (4.31) and (4.32), we get

$$\frac{d}{D'^2}V_O + \frac{D}{D'}v_o - v_c = v_c - v_o$$

$$\frac{d}{D'^2}V_O + \frac{v_o}{D'} = 2v_c$$

$$v_o = 2D'v_c - \frac{d}{D'}V_O. \tag{4.33}$$

Substituting (4.29) into (4.30), we get

$$i_l = i_c + \frac{D}{D'}i_l + \frac{D}{D'}i_c + \frac{d}{D'^2}I_I + i_o$$

$$i_l - \frac{D}{D'}i_l = i_c + \frac{D}{D'}i_c + \frac{d}{D'^2}I_I + i_o$$

$$i_l\frac{D'-D}{D'} = \frac{i_c}{D'} + \frac{d}{D'^2}I_I + \frac{v_o}{Z_x}$$

$$i_l = \frac{1}{D'-D}\frac{v_c}{Z_C} + \frac{d}{D'(D'-D)}I_I + \frac{D'}{D'-D}\frac{v_o}{Z_x}. \tag{4.34}$$

Substituting (4.33) into (4.34), we get

$$i_l = \frac{1}{D'-D}\left[\frac{v_c}{Z_C} + \frac{d}{D'}I_I + \frac{D'}{Z_x}(2D'v_c - \frac{d}{D'}V_O)\right]$$

$$i_l = \frac{1}{D'-D}\Big[\frac{v_c}{Z_c} + \frac{d}{D'}I_I + 2D'^2\frac{v_c}{Z_x} - d\frac{V_O}{Z_x}\Big]. \tag{4.35}$$

By rearranging (4.28), we get

$$v_o(\frac{D}{D'} - 1) + \frac{d}{D'^2}V_O - 2i_l Z_L = 0$$

$$\frac{D'-D}{D'}v_o + \frac{d}{D'^2}V_O - 2i_l Z_L = 0. \tag{4.36}$$

By substituting (4.33) and (4.35) into (4.36), we get

$$\frac{D-D'}{D'}(2D'v_c - \frac{d}{D'}V_O) + \frac{d}{D'^2}V_O$$

$$-2Z_L\Big[\frac{1}{(D'-D)}\frac{v_c}{Z_C}+\frac{d}{D'(D'-D)}I_I+\frac{2D'^2v_c}{(D'-D)Z_x}-\frac{dV_O}{(D'-D)Z_x}\Big]=0$$

$$\Big[\frac{2dV_OZ_L}{(D'-D)Z_x}+\frac{d(D'-D)V_O}{D'^2}+\frac{dV_O}{D'^2}-\frac{2dI_IZ_L}{D'(D'-D)}\Big]$$

$$\Big[-2(D'-D)v_c-\frac{2v_cZ_L}{(D'-D)Z_C}-\frac{4D'^2v_cZ_L}{(D'-D)Z_x}\Big]=0$$

$$d\Big[\frac{2V_OZ_L}{(D'-D)Z_x}+\frac{(D'-D)V_O}{D'^2}+\frac{V_O}{D'^2}-\frac{2I_IZ_L}{D'(D'-D)}\Big]$$

$$=2v_c\Big[(D'-D)+\frac{Z_L}{(D'-D)Z_C}+\frac{2D'^2Z_L}{(D'-D)Z_x}\Big]$$

$$d\Big[\frac{2V_OZ_L}{(D'-D)Z_x}-\frac{2I_IZ_L}{D'(D'-D)}+\frac{V_O(D'-D+1)}{D'^2}\Big]$$

$$=2v_c\Big[(D'-D)+\frac{Z_L}{(D'-D)Z_C}+\frac{2D'^2Z_L}{(D'-D)Z_x}\Big]$$

$$d\Big[\frac{2V_OZ_L}{(D'-D)Z_x}-\frac{2I_IZ_L}{D'(D'-D)}+\frac{2V_O}{D'}\Big]$$

$$=2v_c\Big[(D'-D)+\frac{Z_L}{(D'-D)Z_C}+\frac{2D'^2Z_L}{(D'-D)Z_x}\Big]$$

$$2d\Big[\frac{V_OZ_L}{(D'-D)Z_x}-\frac{I_IZ_L}{D'(D'-D)}+\frac{V_O}{D'}\Big]$$

$$=2v_c\Big[(D'-D)+\frac{Z_L}{(D'-D)Z_C}+\frac{2D'^2Z_L}{(D'-D)Z_x}\Big]$$

$$d\Big[\frac{D'V_OZ_L-I_IZ_LZ_x+V_OZ_x(D'-D)}{D'(D'-D)}\Big]$$

$$=v_c\Big[\frac{(D'-D)^2Z_CZ_x+Z_xZ_L+2D'^2Z_LZ_C}{(D'-D)Z_CZ_x}\Big]$$

$$\frac{v_c}{d}=\Big[\frac{D'V_OZ_L-I_IZ_LZ_x+V_OZ_x(D'-D)}{D'(D'-D)Z_x}\Big]\Big[\frac{(D'-D)Z_CZ_x}{(D'-D)^2Z_CZ_x+Z_xZ_L+2D'^2Z_LZ_C}\Big]$$

$$\frac{v_c}{d}=\Big[\frac{\{D'V_OZ_L-I_IZ_LZ_x+V_OZ_x(D'-D)\}Z_C}{D'(D'-D)^2Z_CZ_x+D'Z_xZ_L+2D'^3Z_LZ_C}\Big].$$

(4.37)

By substituting (4.11), (4.12), and (4.13) into (4.37), we get

$$\frac{v_c}{d}(s)=\frac{\{D'V_OLs-I_ILs(R_x+sL_x)+V_O(D'-D)(R_x+sL_x)\}\frac{1}{sC}}{D'(D'-D)^2(R_x+sL_x)\frac{1}{sC}+D'(R_xsL_x)Ls+2D'^3Ls\frac{1}{sC}}. \tag{4.38}$$

On expanding the numerator and denominator of (4.38) and collecting coefficients of similar powers of 's', we get the control-to-capacitor voltage transfer function

$$Tp = \frac{-I_I L_x L s^2 + (D'V_O L - I_I R_x L + [D' - D]V_O L_x)s + [D' - D]V_O R_x}{D'L_x LCs^3 + D'R_x LCs^2 + (D'[D' - D]^2 L_x + 2D'^3 L)s + D'(D' - D)^2 R_x}. \tag{4.39}$$

4.3.1 Simulation and Experimental Results

Consider an example of the open-loop PWM Z-source converter with the following parameters: $f_s = 40$ kHz, $V_I = 12$ V, $D = 0.3$, $R_x = 50\ \Omega$, $L_x = 330\ \mu$H, $C_1 = C_2 = C = 220\ \mu$F, $L_1 = L_2 = L = 330\ \mu$H. Murata inductor 1433428C with measured ESR of 1.5 Ω at the switching frequency $f_s = 40$ kHz was used for L_1, L_2, and L_x. Electrolytic capacitors with measured capacitance of 220μ F and ESR of 0.2 Ω was used for C_1 and C_2. IRF530N Power MOSFET and U860 ultrafast recovery diode were employed as the switches. IR2110, a high side MOSFET driver was used to trigger the MOSFET. The theoretically predicted Bode plots for $|T_p|$ and ϕ_{T_p} for an ideal PWM Z-source converter (parasitics not included) are shown in Figs. 4.19 and 4.20, respectively. Fig. 4.21 shows the Bode plot obtained by simulating the small-signal model shown in Fig. 4.18 using Saber circuit simulator. The experimental setup used to experimentally obtain T_p is shown in Fig. 4.22 [41]. The parasitic resistances of the inductors and the capacitors are included while predicting the magnitude and phase of T_p by using (4.37). The impedances of the inductors and the capacitors are given by (4.23), (4.24), and (4.25). Op-amp LM357N was used as a comparator to realize a duty-cycle modulator. The duty-cycle modulator has a gain of 20 $\log(1/\mathrm{V_{ref}})$ [1]. The theoretically predicted and experimentally obtained Bode plots for $|T_p|$ and ϕ_{T_p} including the effect of parasitic resistances of the passive components are shown in Figs. 4.23 and 4.24, respectively. In Fig. 4.23, 20 $\log(1/1.75)$ is added to account for the duty-cycle modulator gain. Figs. 4.25 and 4.26 show the theoretically predicted and experimentally obtained response of v_C to step change in D from 0.15 to 0.3,

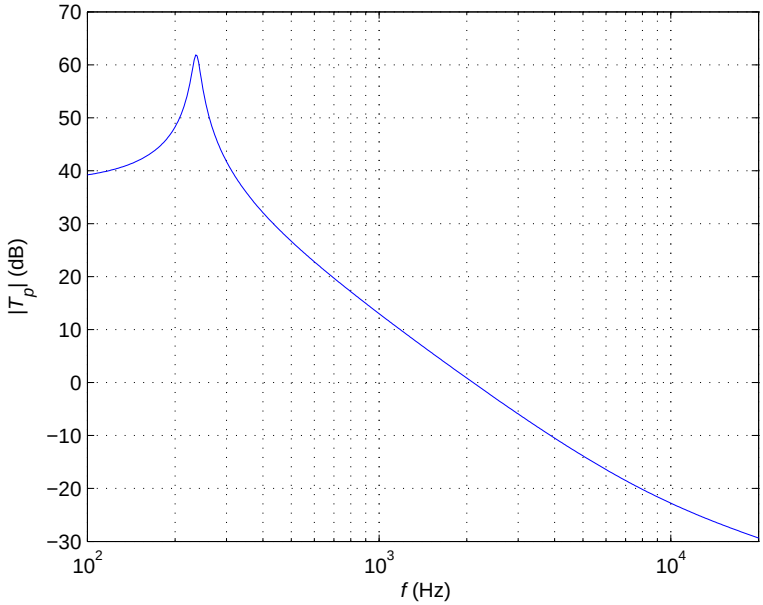

Figure 4.19: Theoretically predicted plot of $|T_p|$ for the lossless PWM Z-source converter operating in CCM.

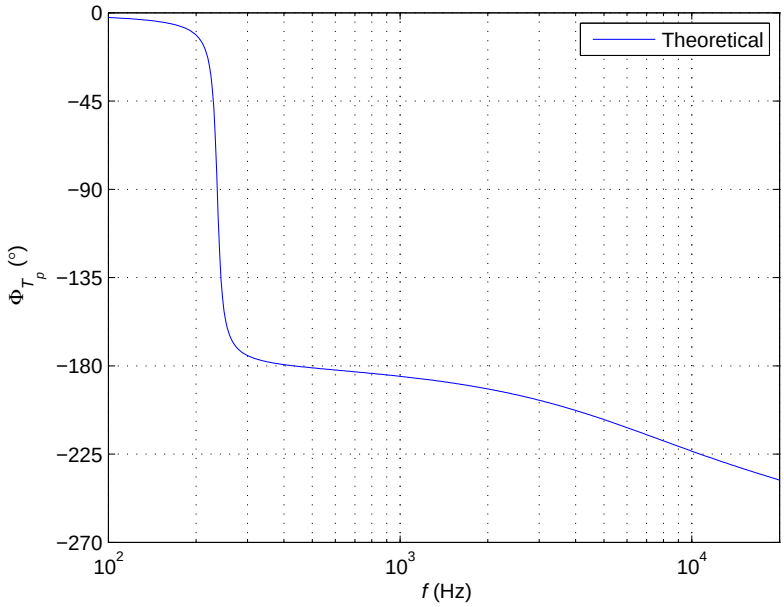

Figure 4.20: Theoretically predicted plot of ϕ_{T_p} for the lossless PWM Z-source converter operating in CCM.

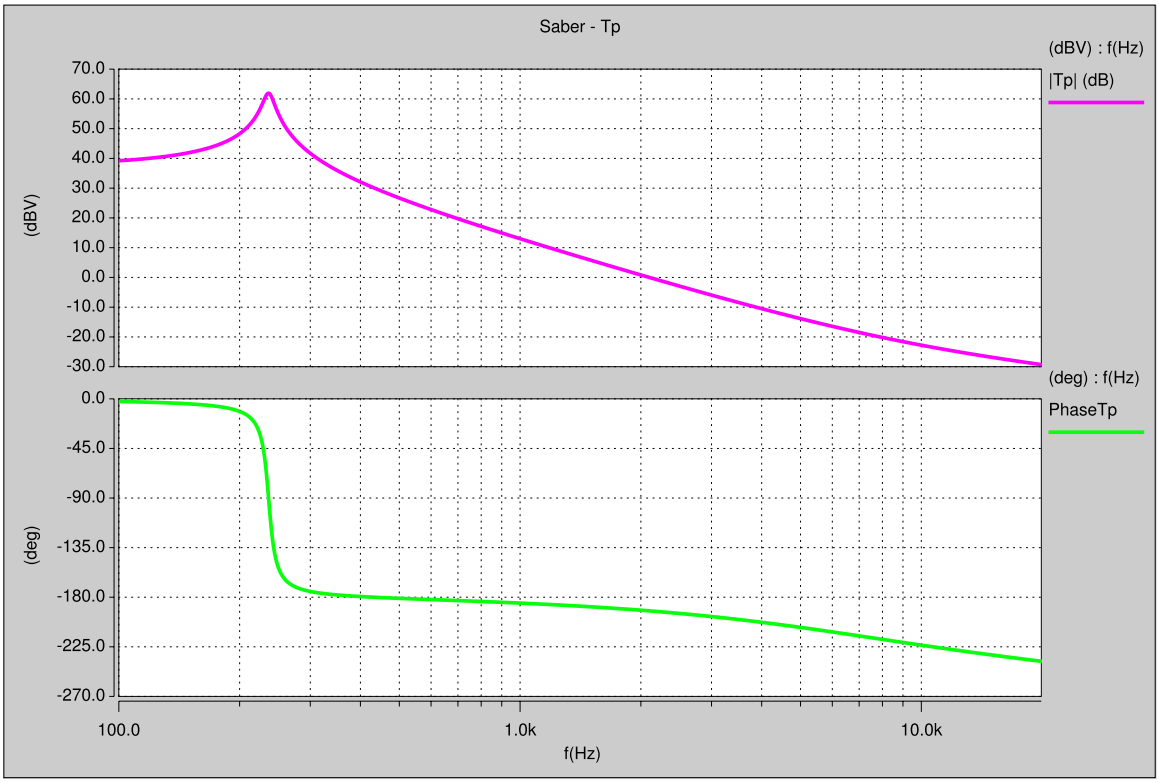

Figure 4.21: Simulated Bode plot of T_p for the lossless PWM Z-source converter operating in CCM.

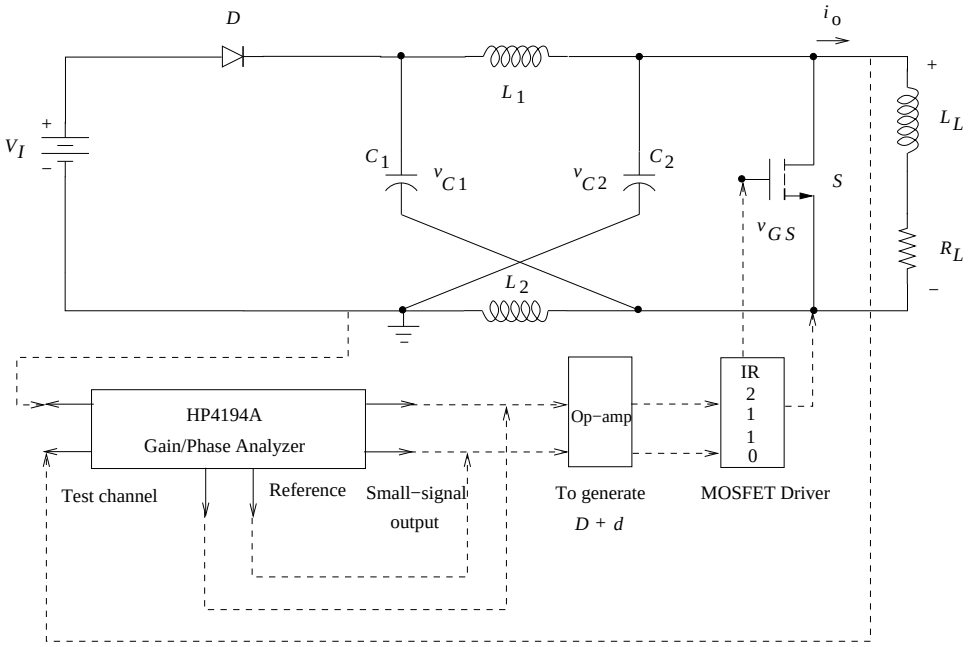

Figure 4.22: Schematic of experimental setup to measure T_p.

respectively.

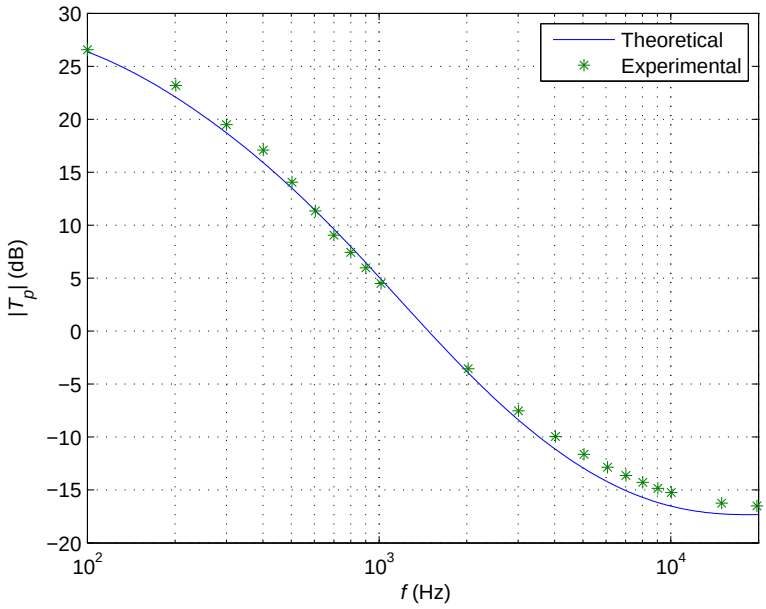

Figure 4.23: Theoretically predicted and experimentally obtained plot of $|T_p|$.

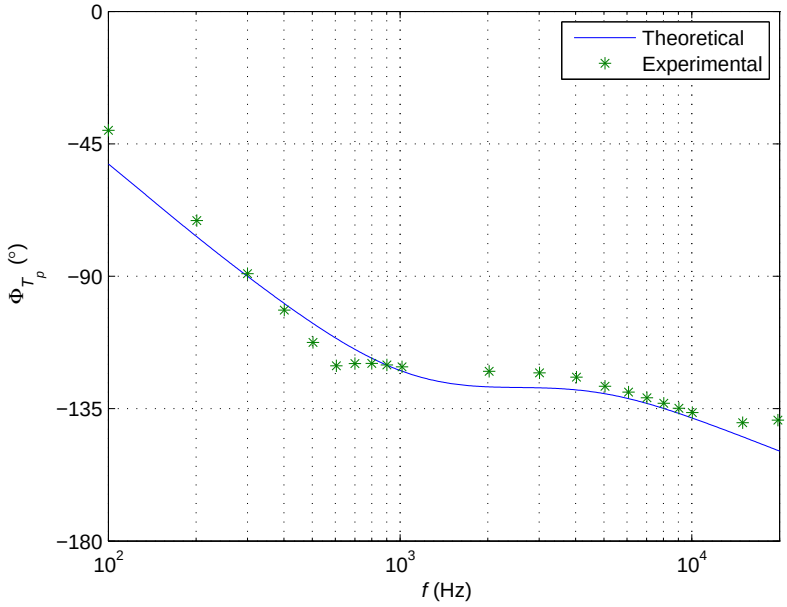

Figure 4.24: Theoretically predicted and experimentally obtained plot of ϕ_{T_p}.

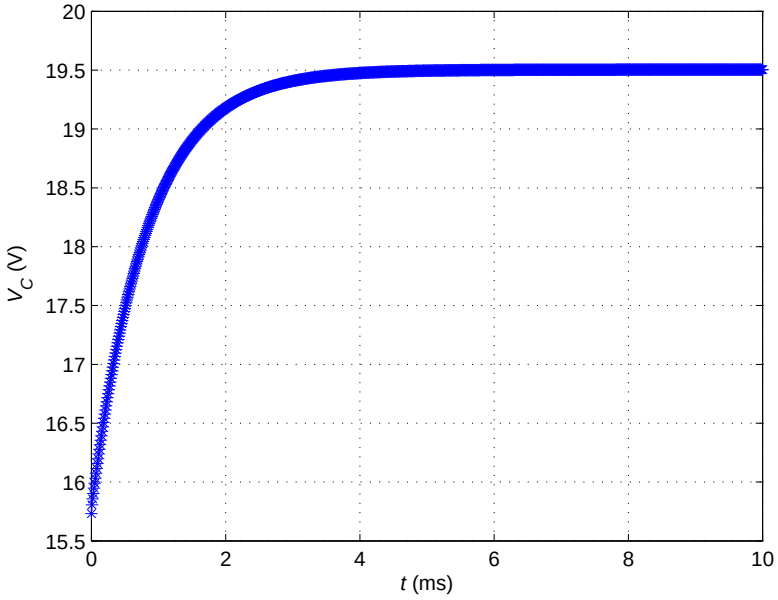

Figure 4.25: Theoretically predicted response in v_C due to a step change in D from 0.15 to 0.3.

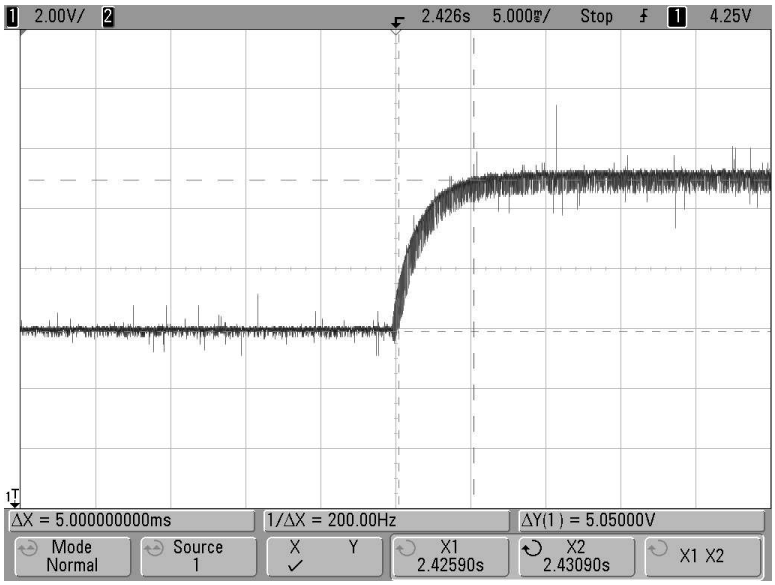

Figure 4.26: Experimentally obtained response in v_C due to a step change in D from 0.15 to 0.3.

4.4 Open-Loop Control-to-Inductor Current Transfer Function

The small-signal model used to derive the open-loop control-to-capacitor voltage transfer function shown in Fig. 4.18 can be employed to derive the open-loop control-to-inductor current transfer function. By Kirchoff's voltage law applied to the inner loop on the input side, inner loop on the load side, and the outer loop, we get

$$\frac{d}{D'^2}V_O + \frac{D}{D'}v_o - i_l Z_L - v_c = 0, \tag{4.40}$$

$$v_c - v_o - i_l Z_L = 0, \tag{4.41}$$

and

$$\frac{d}{D'^2}V_O + \frac{D}{D'}v_o - 2i_l Z_L - v_o = 0, \tag{4.42}$$

respectively. By Kirchoff's current law, we get

$$i_i = i_l + i_c, \tag{4.43}$$

and

$$i_l = i_c + \frac{D}{D'}i_i + \frac{d}{D'^2}I_I + i_o. \tag{4.44}$$

From (4.42), we get

$$v_o = \frac{2D'}{(D - D')}i_l Z_L - \frac{V_O d}{D'(D' - D)}. \tag{4.45}$$

By substituting (4.43) in (4.44), we get

$$i_c = (D' - D)i_l - \frac{d}{D'}I_I - \frac{D'v_o}{Z_x}. \tag{4.46}$$

Substituting (4.45) and (4.46) in (4.40), we get

$$\frac{i_l}{d} = \frac{-V_O Z_x + (D - D')I_I Z_C Z_x - D'V_O Z_C}{D'(D' - D)Z_L Z_x - 2DD'Z_L Z_x - D'(D - D')^2 Z_C Z_x - 2D'^3 Z_L Z_C}. \tag{4.47}$$

By substituting (4.11), (4.12), and (4.13) into (4.47), we get

$$T_{pi}(s) = \frac{i_l(s)}{d(s)} =$$

$$\frac{-V_O LCs^2 + (D - D')I_I L_x s + (D - D')I_I R_x - V_O R_x - D'V_O}{(D'(D - D') - 2DD')[L_x LCs^3 + R_x LCs^2] - (D'(D - D')^2 L_x - 2D1^3 L)s - D'(D - D')^2 R_x}. \tag{4.48}$$

4.4.1 Simulation and Experimental Results

Consider an example of the open-loop PWM Z-source converter with the following parameters: $f_s = 40$ kHz, $V_I = 12$ V, $D = 0.3$, $R_x = 50\ \Omega$, $L_x = 330\ \mu$H, $C_1 = C_2 = C = 220\ \mu$F, $L_1 = L_2 = L = 330\ \mu$H. Murata inductor 1433428C with measured ESR of 1.5 Ω at the switching frequency $f_s = 40$ kHz was used for L_1, L_2, and L_x. Electrolytic capacitors with measured capacitance of 220μ F and ESR of 0.2 Ω was used for C_1 and C_2. IRF530N Power MOSFET and U860 ultrafast recovery diode were employed as the switches. IR2110, a high side MOSFET driver was used to trigger the MOSFET. The theoretically predicted Bode plots for $|T_{pi}|$ and $\phi_{T_{pi}}$ for an ideal PWM Z-source converter (parasitics not included) are shown in Figs. 4.27 and 4.28, respectively. Fig. 4.29 shows the Bode plot obtained by simulating the small-signal model shown in Fig. 4.18 using Saber circuit simulator. The experimental setup used to experimentally obtain T_{pi} is shown in Fig. 4.22 [41]. The parasitic resistances of the inductors and the capacitors are included while predicting the magnitude and phase of T_{pi} by using (4.47). The impedances of the inductors and the capacitors are given by (4.23), (4.24), and (4.25). Op-amp LM357N was used as a comparator to realize a duty-cycle modulator. The duty-cycle modulator has a gain of 20 $\log(1/\mathrm{V_{ref}})$ [1]. The theoretically predicted and experimentally obtained Bode plots for $|T_{pi}|$ and $\phi_{T_{pi}}$ including the effect of parasitic resistances of the passive components are shown in Figs. 4.31 and 4.32, respectively. In Fig. 4.31, 20 $\log(1/1.75)$ is added to account for the duty-cycle modulator gain. Figs. 4.33 and 4.34 show the theoretically predicted and experimentally obtained response of i_L to step change in D from 0.15 to 0.3, respectively.

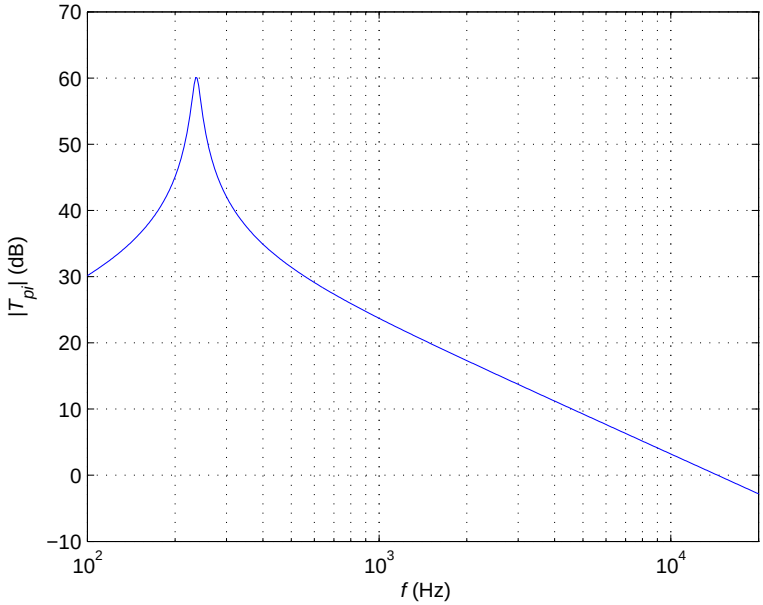

Figure 4.27: Theoretically predicted plot of $|T_{pi}|$ for the lossless PWM Z-source converter operating in CCM.

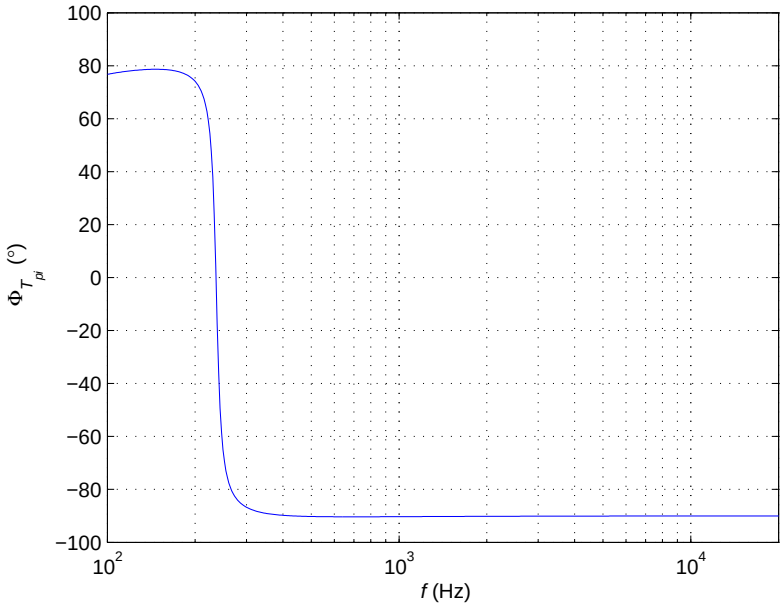

Figure 4.28: Theoretically predicted plot of $\phi_{T_{pi}}$ for the lossless PWM Z-source converter operating in CCM.

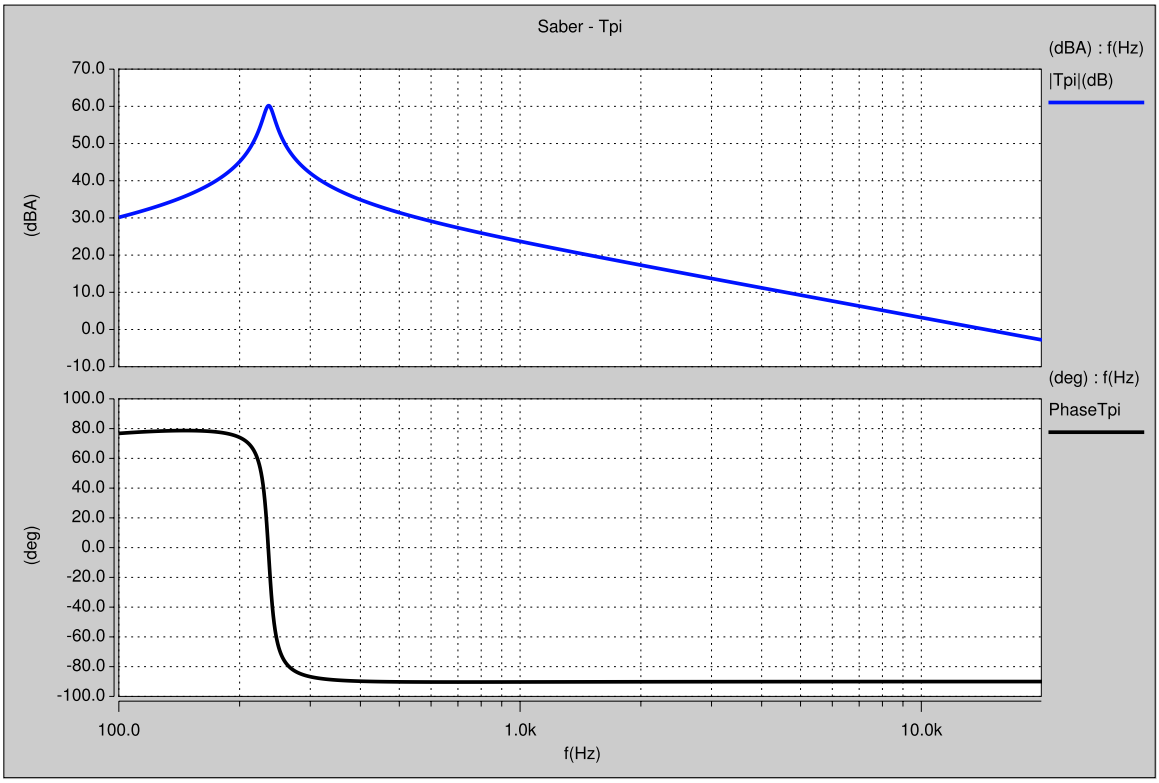

Figure 4.29: Simulated Bode plot of T_{pi} for the lossless PWM Z-source converter operating in CCM.

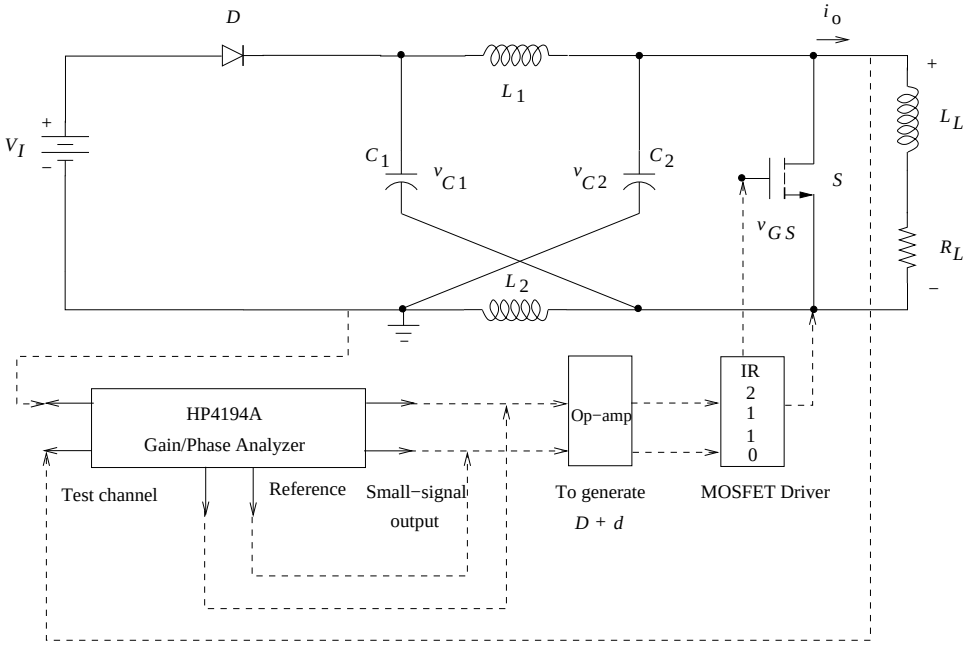

Figure 4.30: Schematic of experimental setup to measure T_{pi}.

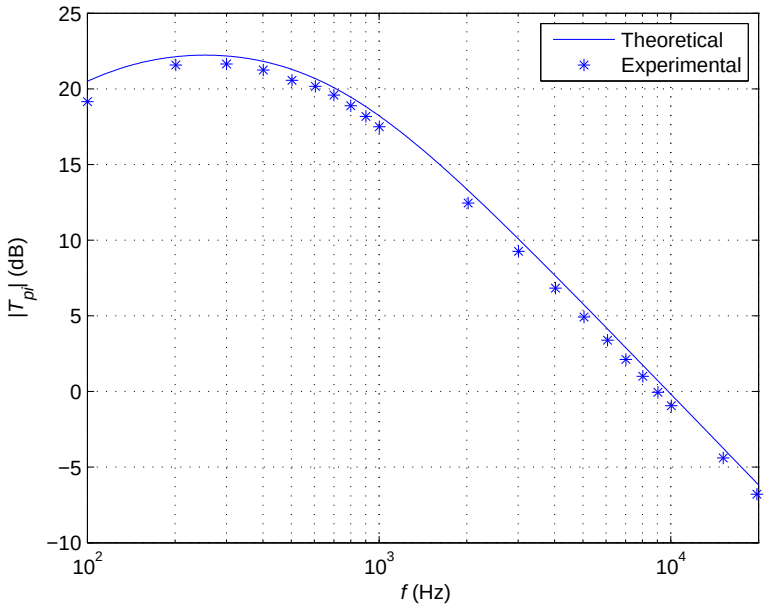

Figure 4.31: Theoretically predicted and experimentally obtained plot of $|T_{pi}|$.

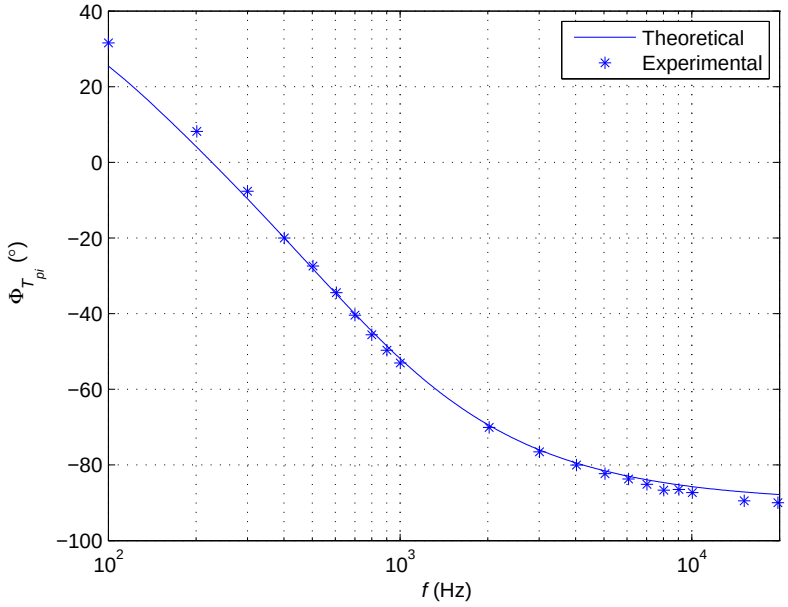

Figure 4.32: Theoretically predicted and experimentally obtained plot of $\phi_{T_{pi}}$.

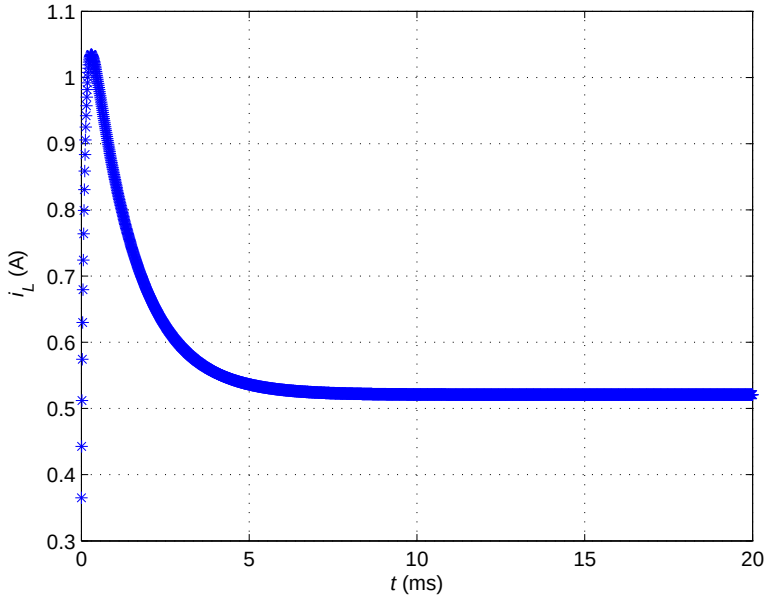

Figure 4.33: Theoretically predicted response in i_L due to a step change in D from 0.15 to 0.3.

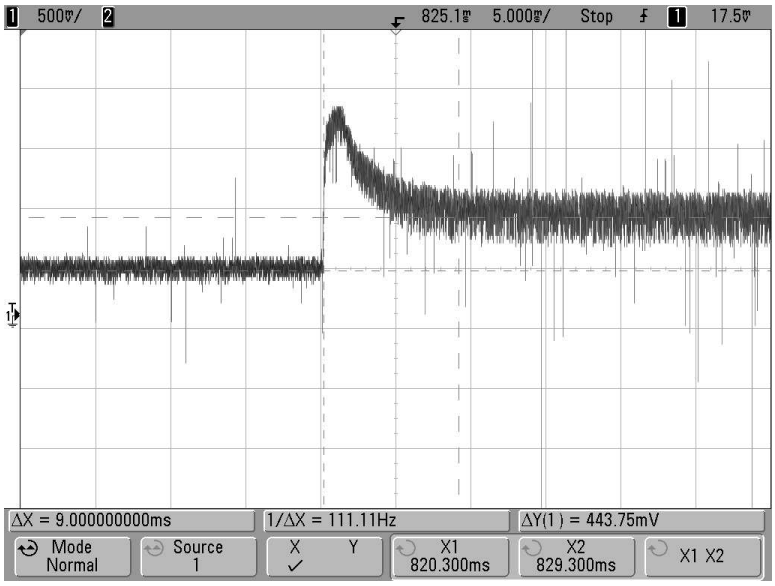

Figure 4.34: Experimentally obtained response in i_L due to a step change in D from 0.15 to 0.3.

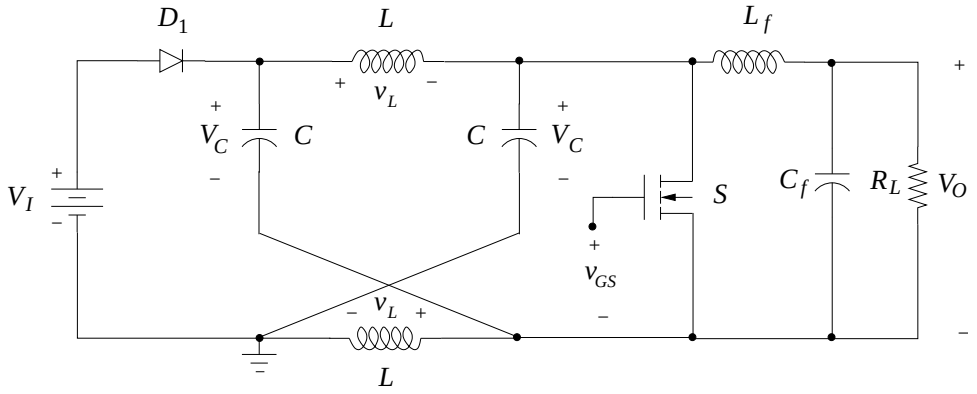

Figure 5.1: PWM Z-source dc-dc converter.

5 Steady-State Analysis of PWM Z-source dc-dc Converter in CCM

The PWM Z-source dc-dc converter is a boost converter. The PWM Z-source dc-dc converter shown in Fig. 5.1 consists of a diode D_1, two identical inductors denoted by L and two identical capacitors denoted by C connected in a manner to obtain the unique impedance or Z-network, an active switch S such as a MOSFET/IGBT, a second order low-pass filter formed by L_f and C_f, and the resistive load R_L.

The objectives of this chapter are to present (1) the equivalent circuits and the associated expressions corresponding to different stages of operation of the PWM Z-source dc-dc converter in CCM, (2) the dc input-to-output voltage conversion factor and minimum inductance required to ensure CCM operation (3) equations for power losses in the components of the PWM Z-source dc-dc converter and the overall efficiency (4) output voltage ripple across the filter capacitor C_f and its ESR r_{C_f} and (4) experimental results to validate the theoretical analysis. This work is published in [21].

5.1 Idealized Waveforms

The following assumptions are used in the present analysis.

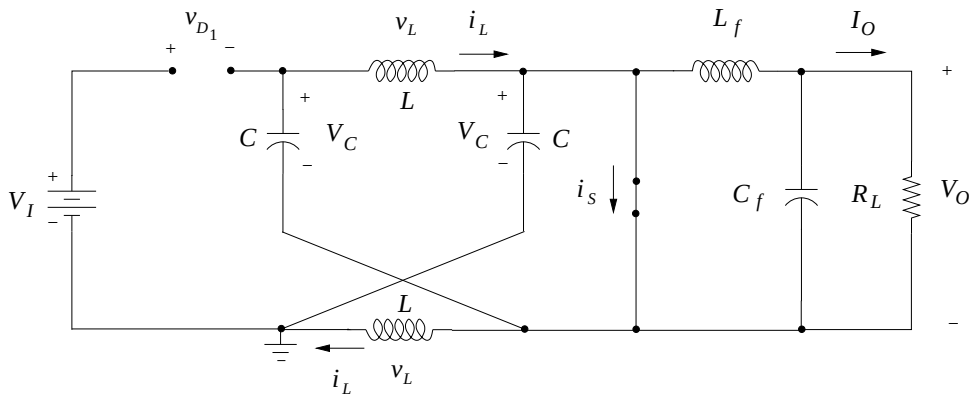

Figure 5.2: Equivalent circuit of the PWM Z-source dc-dc converter when S is ON and D_1 is OFF.

1. Inductors, capacitors, and resistors are linear, time-invariant, and frequency independent.

2. Semiconductor switches, i.e., the MOSFET and the diode are ideal (except in estimating efficiency).

3. The natural time constant of the converter is much longer than one switching time period.

Referring to Fig. 5.1, the MOSFET S is switched at a constant frequency $f_s = 1/T$ with the duty ratio of S given by $D = t_{on}/T$, where t_{on} is the duration when S is in the ON position. Since the MOSFET S and the diode D_1 have complimentary duty ratios, the duty ratio of the diode D_1 is given by $1 - D$. Due to the symmetry of the Z-network, and since $L_1 = L_2 = L$ and $C_1 = C_2 = C$, we have $i_{L_1} = i_{L_2} = i_L$, $v_{L_1} = v_{L_2} = v_L$, and $v_{C_1} = v_{C_2} = v_C$.

5.1.1 Time Interval: $0 \leq t \leq DT$

The equivalent circuit corresponding to this state is shown in Fig. 5.2. In this state, the voltage across the diode is $V_I - 2V_C$, causing the diode to be reverse biased or OFF. Shorting the output terminals results in the diode D_1 being reverse biased, thus isolating the energy source V_I from the rest of the circuit. The current through the

diode and the voltage across the MOSFET are zero, i.e., $i_{D_1} = 0$ and $v_S = 0$. The voltage across the inductor v_L is

$$v_L = 2V_C - V_C = V_C = L\frac{di_L}{dt}. \tag{5.1}$$

The inductor current i_L is given by

$$\begin{aligned} i_L(t) &= \frac{1}{L}\int_0^t v_L dt + i_L(0) \\ &= \frac{V_C}{L}t + i_L(0). \end{aligned} \tag{5.2}$$

Hence, the peak inductor current which occurs at $t = DT$ is given by

$$i_L(DT) = \frac{V_C}{L}(DT) + i_L(0). \tag{5.3}$$

The peak-to-peak value of the inductor current is expressed as

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_C D}{f_s L}. \tag{5.4}$$

By KCL, the current through the switch S is given by $i_S = 2i_L - I_O$. The output voltage across the load resistor R_L is maintained by the output capacitor C_f. The voltage across the output filter inductor v_{L_f} is given by

$$v_{L_f} = -V_O = L_f\frac{di_{L_f}}{dt}. \tag{5.5}$$

The resulting current through i_{L_f} is

$$\begin{aligned} i_{L_f} &= \frac{1}{L_f}\int_0^t v_{L_f} dt + i_{L_f}(0) \\ &= \frac{-V_O}{L_f}(t) + i_{L_f}(0). \end{aligned} \tag{5.6}$$

By letting $t = DT$ in (5.6), we obtain

$$i_{L_f(peak)} = i_{L_f}(DT) = \frac{-V_O}{L_f}(DT) + i_{L_f}. \tag{5.7}$$

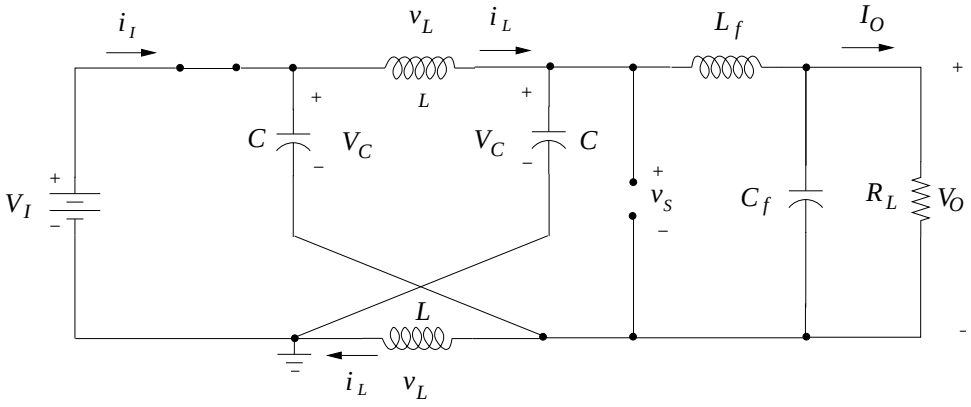

Figure 5.3: Equivalent circuit of the PWM Z-source dc-dc converter when S is OFF and D is ON.

The peak-to-peak value of the current flowing through the filter inductor is

$$\Delta i_{L_f} = i_{L_f}(0) - i_{L_f}(DT). \tag{5.8}$$

Using (5.7) in (5.8), we have

$$\Delta i_{L_f} = \frac{DV_O}{f_s L_f}. \tag{5.9}$$

5.1.2 Time Interval: $DT \leq t \leq T$

The equivalent circuit corresponding to the state when the MOSFET S is OFF and the diode D_1 is forward biased is shown in Fig. 5.3. In this state, the Z-network acts as the interface between the source and the load. The voltage across the diode v_{D_1} and the current through the MOSFET i_S are zero. The voltage across the inductor v_L is given by

$$v_L = V_I - V_C = \frac{di_L}{dt}. \tag{5.10}$$

The current through the inductor i_L is given by

$$\begin{aligned} i_L(t) &= \frac{1}{L}\int_{DT}^{t} v_L dt + i_L(DT) \\ &= \frac{V_I - V_C}{L}(t - DT) + i_L(DT). \end{aligned} \tag{5.11}$$

The inductor current at $t = T$ is given by

$$i_L(T) = \frac{V_I - V_C}{L} T(1 - D) + i_L(DT). \tag{5.12}$$

The voltage across L_f is given by

$$v_{L_f} = V_O - V_I = L_f \frac{di_{L_f}}{dt}. \tag{5.13}$$

The resulting current through L_f is given by

$$i_{L_f} = \frac{1}{L_f} \int_{DT}^{t} v_{L_f} + i_{L_f}(DT). \tag{5.14}$$

By using (5.13) and (5.14), we obtain

$$i_{L_f} = \frac{V_O - V_I}{L_f}(t - DT) + i_{L_f}(DT). \tag{5.15}$$

By letting $t = T$ in (5.15), we obtain the peak output inductor current to be

$$i_{L_f(peak)} = \frac{V_O - V_I}{L_f} T(1 - D) + i_{L_f}(DT). \tag{5.16}$$

The peak-to-peak value of the current through the filter inductor is given by

$$\begin{aligned} \Delta i_{L_f} &= i_{L_f}(T) - i_{L_f}(DT) \\ &= \frac{V_O - V_I}{L_f} T(1 - D). \end{aligned} \tag{5.17}$$

Fig. 5.4 shows the idealized theoretical waveforms for the PWM Z-source dc-dc converter.

5.2 DC Voltage conversion factor and Minimum Inductance for CCM

5.2.1 DC Voltage Conversion Factor for CCM

By the volt-second balance property of the inductor L, the average voltage across an inductor in steady state is zero. From (5.1) and (5.10), the volt-second balance for the inductor L can be expressed as

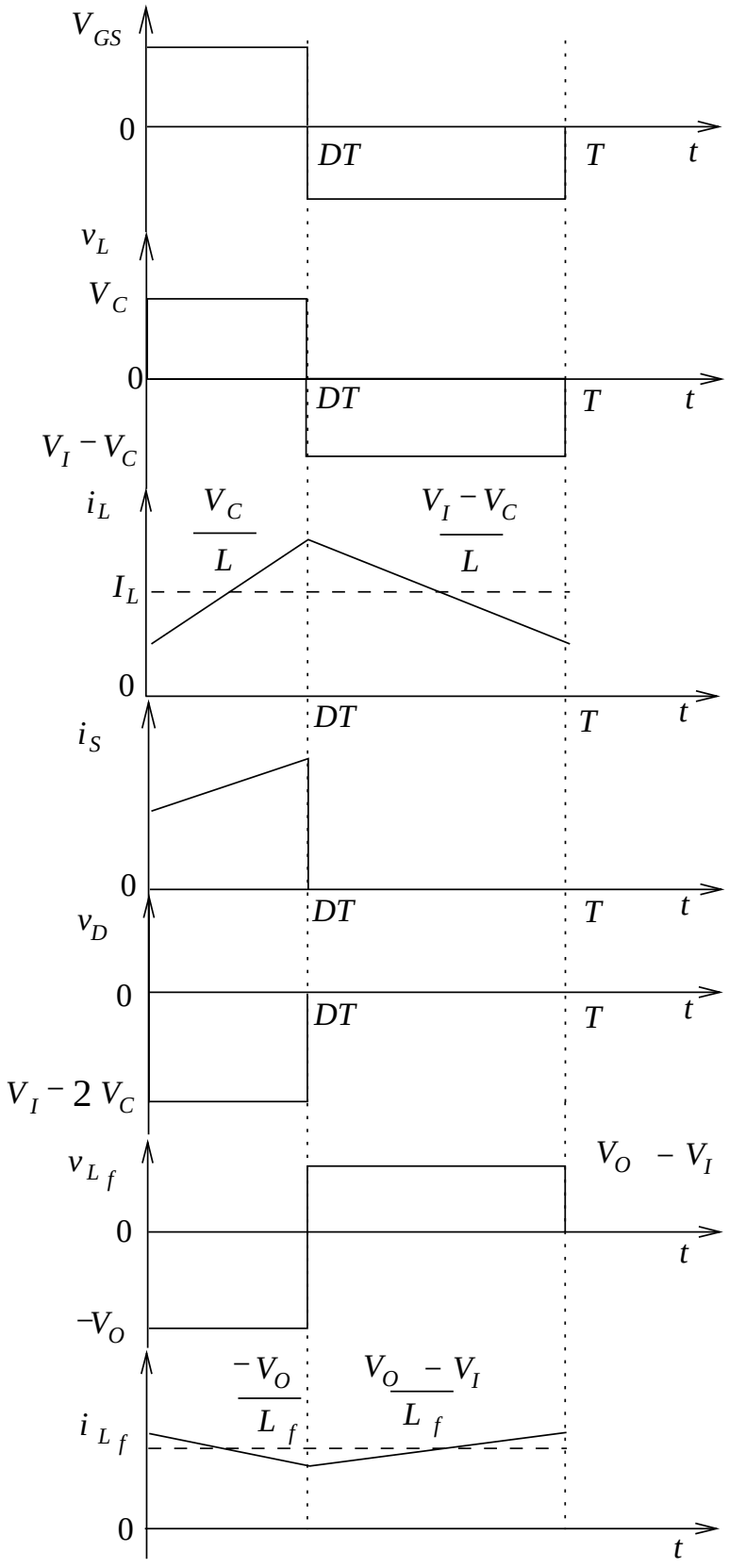

Figure 5.4: Voltage and current waveforms of the PWM Z-source dc-dc converter for CCM.

$$\int_0^{DT} v_L(t)dt + \int_{DT}^{T} v_L(t)dt = 0. \tag{5.18}$$

Thus,

$$V_C DT + (V_I - V_C)(1-D)T = 0, \tag{5.19}$$

which gives

$$\frac{V_C}{V_I} = \frac{1-D}{1-2D}. \tag{5.20}$$

Equation (5.20) is the dc input-to-capacitor voltage conversion factor [6], [31] - [33]. Referring to Fig. (5.1), by applying KVL to the loop containing the Z-network capacitor C, the filter inductor L_f, the parallel combination of $R_L||C_f$, and the Z-network inductor L, we obtainfering to Fig. (5.1), by applying KVL to the loop containing the Z-network capacitor C, the filter inductor L_f, the parallel combination of $R_L||C_f$, and the Z-network inductor L, we obtain

$$V_C - v_{L_f} - V_O - v_L = 0. \tag{5.21}$$

Since the average values of $v_{L_f} = 0$ and $v_L = 0$, (5.21) leads to

$$V_C = V_O. \tag{5.22}$$

Using (5.20) and (5.22), we derive the dc input-to-output voltage conversion factor as

$$M_{VDC} = \frac{V_O}{V_I} = \frac{1-D}{1-2D}. \tag{5.23}$$

Since $V_I I_I = V_O I_O$ for a lossless converter, the dc input-to-output current conversion factor can be expressed as

$$M_{IDC} = \frac{I_O}{I_I} = \frac{1-2D}{1-D}. \tag{5.24}$$

5.2.2 Minimum Inductance for CCM

This part of the work is based on [1]. From (5.1) and (5.22), the peak inductor current is

$$i_L(DT) = \frac{V_O D}{f_s L} + i_L(0). \tag{5.25}$$

At the boundary between continuous conduction mode and discontinuous conduction mode (CCM/DCM), we have $i_L(0) = 0$. Hence, the peak inductor current at the CCM/DCM boundary is

$$\Delta i_L = i_L(DT) = \frac{V_O D}{f_s L}. \tag{5.26}$$

Since the dc inductor current is equal to the dc input current, at the CCM/DCM boundary we have

$$I_{LB} = I_{IB} = \frac{\Delta i_L}{2} = \frac{V_O D}{2 f_s L}. \tag{5.27}$$

Using (5.24) and (5.27), we derive the output current at the CCM/DCM boundary to be

$$I_{OB} = \frac{D(1-2D)V_O}{2(1-D)f_s L}. \tag{5.28}$$

The load resistance at the CCM/DCM boundary can be expressed as

$$R_{LB} = \frac{2(1-D)f_s L}{D(1-2D)}. \tag{5.29}$$

Figs. 5.5 and 5.6 show the plots of normalized load current I_{OB} and normalized load resistance R_{LB} as a function of D at the CCM/DCM boundary, respectively. Setting the derivative of I_{OB} to zero in (5.28), we obtain

$$\frac{dI_{OB}}{dD} = \frac{V_O}{2 f_s L}(2D^2 - 4D + 1) = 0. \tag{5.30}$$

From (5.30), the maximum value of I_{OB} occurs at $D = 0.292$. By substituting $D = 0.292$ in (5.28), we obtain

$$I_{OBmax} = 0.0858 \frac{V_O}{f_s L_{min}} \tag{5.31}$$

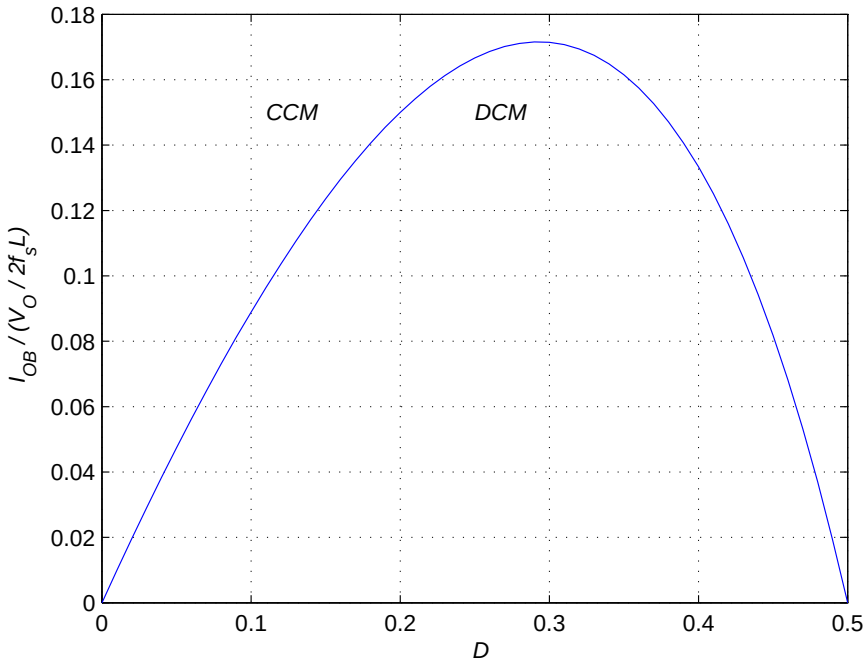

Figure 5.5: Normalized load current $I_{OB}/(V_O/2f_sL)$ as a function of D at the CCM/DCM boundary for PWM Z-source dc-dc converter.

or

$$L_{min} = 0.0858\frac{V_O}{f_s I_{OBmax}}. \tag{5.32}$$

Using $I_{OBmax} = I_{Omin} = V_O/R_{Lmax}$ in (5.31), we determine the minimum inductance for CCM operation to be

$$L > L_{min} = 0.0858\frac{R_{Lmax}}{f_s}. \tag{5.33}$$

5.3 Output Voltage Ripple in PWM Z-source dc-dc Converter in CCM

The output circuit of the PWM Z-source dc-dc converter is shown in Fig. 5.7. Here, the filter capacitor is modeled as an ideal capacitor C_f and its equivalent series resistance (ESR) r_{C_f}. The dc component of the current through the filter inductor

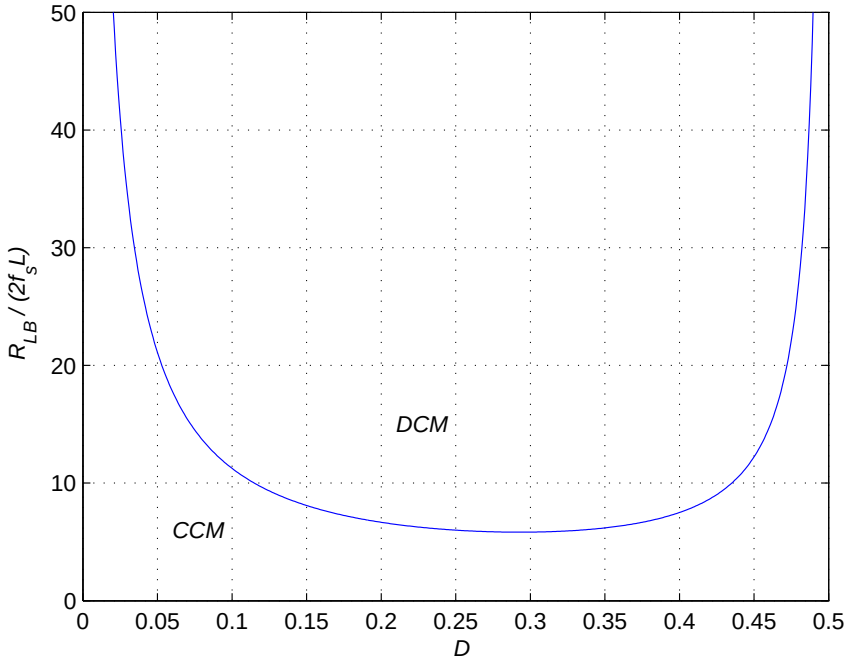

Figure 5.6: Normalized load resistance $R_{LB}/(2f_sL)$ as a function of D at the CCM/DCM boundary for PWM Z-source dc-dc converter.

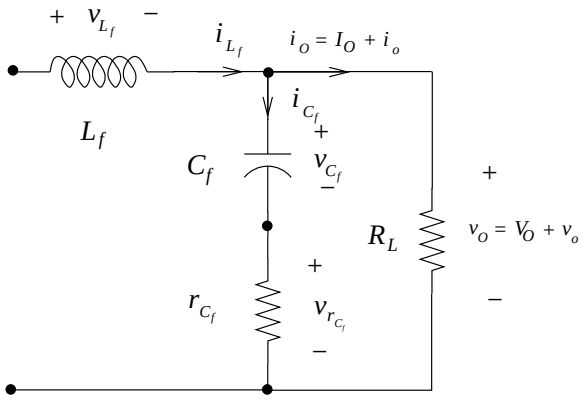

Figure 5.7: Output circuit of the PWM Z-source dc-dc converter.

I_{L_f} flows through the load resistor R_L while the ac component i_{C_f} flows through the filter capacitor. This part of the work is based on [1]. Consider the time interval $0 \leq t \leq DT$. The current through the filter capacitor is given by

$$i_{C_f} = \frac{-V_O}{L_f}(t) + \frac{\Delta i_{L_f}}{2}. \tag{5.34}$$

Using (5.9) and (5.34), we have

$$i_{C_f} = \frac{-\Delta i_{L_f}}{DT}(t) + \frac{\Delta i_{L_f}}{2}. \tag{5.35}$$

The voltage across the ESR r_{C_f} of the filter capacitor C_f is given by

$$v_{r_{C_f}} = i_{C_f} r_{C_f} = -\Delta i_{L_f} r_{C_f}\Big(\frac{t}{DT} - \frac{1}{2}\Big). \tag{5.36}$$

The voltage across the filter capacitor C_f is given by

$$v_{C_f} = \frac{1}{C_f}\int_0^t i_{C_f} dt + v_{C_f}(0). \tag{5.37}$$

Using (5.35) in (5.37), we obtain

$$v_{C_f} = \frac{-\Delta i_{L_f}}{2C_f}\Big(\frac{t^2}{DT} - t\Big) + v_{C_f}(0). \tag{5.38}$$

The ac component of the output voltage is the sum of voltages across C_f and r_{C_f}, and is given by

$$v_O = v_{r_{C_f}} + v_{C_f} =$$
$$-\Delta i_{L_f}\Big(\frac{t^2}{2C_f DT} + \frac{r_{C_f}}{DT}t - \frac{1}{2C_f}t - \frac{r_{C_f}}{2}\Big) + v_{C_f}(0). \tag{5.39}$$

Setting the derivative of v_O to zero, the time instant at which the maximum value of v_O occurs is

$$t_{max} = \frac{DT}{2} - C_f r_{C_f}. \tag{5.40}$$

The maximum value of v_O occurs at $t = 0$, hence by letting $t = 0$ in (5.40), we obtain

$$\frac{DT}{2} = C_f r_{C_f}. \tag{5.41}$$

The maximum value of v_O is equal to the maximum value of $v_{r_{Cf}}$. This occurs at a minimum value of C_f, which can be found from (5.41), and is

$$C_{min(off)} = \frac{D_{max}}{2 f_s r_{C_f(max)}}. \tag{5.42}$$

Consider the time interval $DT \leq t \leq T$. The current through the filter capacitor is

$$i_{C_f} = \frac{V_O - V_I}{L_f}(t - DT) - \frac{\Delta i_{L_f}}{2}. \tag{5.43}$$

From (5.17) and (5.43) we obtain

$$i_{C_f} = \frac{\Delta i_{L_f}}{T(1-D)}(t - DT) - \frac{\Delta i_{L_f}}{2}. \tag{5.44}$$

The voltage across r_{C_f} can be expressed as

$$v_{r_{C_f}} = r_{C_f}\Delta i_{L_f}\Big[\frac{(t - DT)}{T(1-D)} - \frac{1}{2}\Big]. \tag{5.45}$$

The voltage across the filter capacitor C_f is given by

$$v_{C_f} = \frac{1}{C_f}\int_{DT}^{t} i_{C_f}dt + v_{C_f}(DT). \tag{5.46}$$

Using (5.44) and (5.46), we obtain

$$\begin{aligned} v_{C_f} = \frac{-\Delta i_{L_f}}{2C_f}\Big[\frac{-t^2 - 2DTt + (DT)^2}{(1-D)T} + (t - DT)\Big] \\ + v_{C_f}(DT) \end{aligned} \tag{5.47}$$

The ac component of the output voltage is the sum of the voltages across C_f and r_{C_f}, and is

$$\begin{aligned} v_O = -r_{C_f}\Delta i_{L_f}\Big[\frac{-(t - DT)}{T(1-D)} + \frac{1}{2}\Big] \\ \frac{-\Delta i_{L_f}}{2C_f}\Big[\frac{-t^2 - 2DTt + (DT)^2}{(1-D)T} + (t - DT)\Big] \\ + v_{C_f}(DT). \end{aligned} \tag{5.48}$$

Setting the derivative of v_O with respect to time to zero, we determine the time instant corresponding to a minimum value of v_O, and is expressed as

$$t_{min} = \frac{(1+D)T}{2} - C_f r_{C_f}. \tag{5.49}$$

The minimum value of v_O is equal to the minimum value of $v_{r_{C_f}}$, and it occurs at $t_{min} = DT$. Hence, by letting $t = DT$ in (5.49), we obtain

$$t_{min} = \frac{(1+D)T}{2} - C_f r_{C_f} = DT. \tag{5.50}$$

The value of t_{min} corresponding to (5.50) occurs at a minimum capacitance given by

$$C_{(min)on} = \frac{(1-D_{min})}{2f_s r_{C_f(max)}}. \tag{5.51}$$

Hence, the peak-to-peak value of the output voltage ripple is independent of the voltage across the filter capacitor C_f and is determined only by the voltage across the ESR of the filter capacitor r_{C_f} if

$$C_f \geq max\ \{C_{(min)on},\ C_{(min)off}\}. \tag{5.52}$$

The minimum value of filter capacitances can be segregated as

$$C_{min} = \frac{D_{max}}{2f_s r_C} \quad \text{for} \quad (D_{min} + D_{max}) > 1 \tag{5.53}$$

and

$$C_{min} = \frac{1-D_{min}}{2f_s r_C} \quad \text{for} \quad (D_{min} + D_{max}) < 1. \tag{5.54}$$

If the condition specified in (5.52) is satisfied, the peak-to-peak output voltage ripple is

$$v_{O(p-p)} = r_{C_f} \Delta i_{L(max)} = \frac{r_{C_f} V_O D}{f_s L_f}. \tag{5.55}$$

If the condition specified in (5.52) is not satisfied, both $V_{C_f(p-p)}$ and $v_{r_{Cf}(p-p)}$ will contribute to the output voltage ripple. The output voltage ripple v_O and the associated value of the filter capacitance C_f is estimated as follows. The maximum increase of the charge stored in the filter capacitor in each switching cycle is

$$\Delta Q = \frac{\frac{T}{2}\frac{\Delta i_{L_f(max)}}{2}}{2} = \frac{\Delta i_{L_f(max)}}{8 f_s}. \tag{5.56}$$

The peak-to-peak voltage across the capacitor is

$$v_{C_f(p-p)} = \frac{\Delta Q}{C_f} = \frac{\Delta i_{L_f(max)}}{8 f_s C_f} = \frac{V_O D}{8 L_f f_s^2 C_f}. \tag{5.57}$$

Since $f_o = 1/2\pi\sqrt{L_f C_f}$ is the corner frequency of the output filter, then (5.57) can be expressed as

$$v_{C_f(p-p)} = \frac{V_O D \pi^2 {f_o}^2}{2 {f_s}^2}. \tag{5.58}$$

Hence, the total output voltage ripple is

$$v_{O(p-p)} = v_{C_f(p-p)} + v_{r_{C_f}(p-p)}, \tag{5.59}$$

where $v_{r_{C_f}(p-p)} = r_{C_f} \Delta i_{L_f(max)}$. Fig. 5.8 shows the voltage and current waveforms associated with the filter capacitor C_f and its ESR r_{C_f}.

5.4 Power Losses and dc Voltage conversion factor of a Non-Ideal PWM Z-source dc-dc Converter

Equivalent circuit of PWM Z-source dc-dc converter with parasitic resistances is shown in Fig. 5.9. The diode is represented by an ideal switch in series with a resistor R_F representing the forward resistance and a voltage source V_F representing the forward voltage drop. The MOSFET is replaced by an ideal switch in series with its equivalent drain-source resistance represented by r_{DS}. The ESRs of the inductors and capacitors have been included to account for parasitic resistance of the passive components. This part of the work is based on [1]. The power loss in the individual components of the Z-source dc-dc converter are estimated below

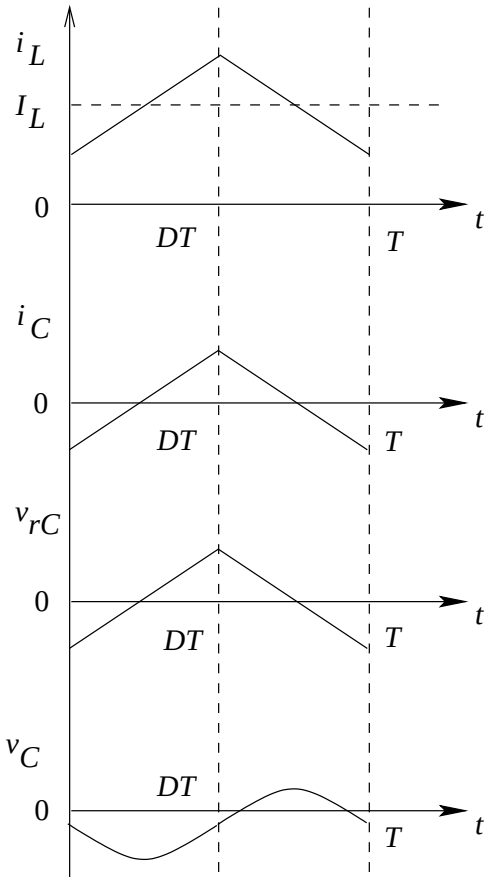

Figure 5.8: Ripple voltage in PWM Z-source dc-dc converter.

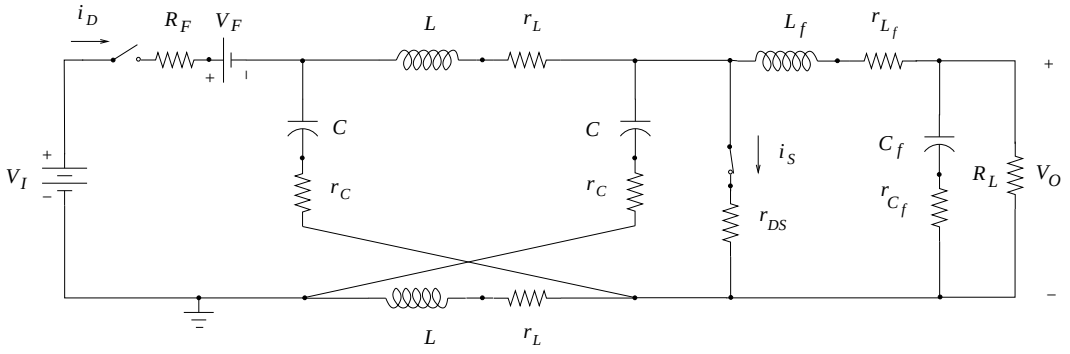

Figure 5.9: PWM Z-source dc-dc converter with parasitic resistances.

5.4.1 Losses in Semiconductor Switches

By KCL, and noting that $I_I = I_L$, the current through the MOSFET S is

$$i_S = \begin{cases} 2I_L - I_O = 2I_I - I_O, & 0 < t \leq DT \\ 0, & DT < t \leq T \end{cases} . \tag{5.60}$$

Using (5.24) in (5.60), the root mean square value is

$$i_{S(RMS)} = \frac{I_O}{1-2D}\sqrt{D}. \tag{5.61}$$

Hence, the Ohmic power loss in MOSFET S is

$$\begin{aligned} P_{r_{DS}} = {I_{S(RMS)}}^2 r_{DS} &= \frac{I_O^2}{(1-2D)^2} D r_{DS} \\ &= \frac{P_O D r_{DS}}{(1-2D)^2 R_L}, \end{aligned} \tag{5.62}$$

where r_{DS} is the MOSFET on-resistance, P_O is output power, and R_L is the load resistance. Assuming the output capacitance of the MOSFET S to be linear, the switching loss in the converter is

$$P_{sw} = \frac{f_s C_f V_O^2}{2} = \frac{f_s C_f P_O R_L}{2}, \tag{5.63}$$

where C_f is the output capacitance of the MOSFET S. The total power loss in the MOSFET is the sum of the switching power loss and the conduction power loss. By (5.62) and (5.63), we obtain

$$P_{FET} = P_{r_{DS}} + P_{sw} = \Big[\frac{D r_{DS}}{(1-2D)^2 R_L} + \frac{f_s C_f R_L}{2}\Big] P_O. \tag{5.64}$$

The current through the diode D is

$$i_D = \begin{cases} 0, & \text{for} \quad 0 < t \le DT \\ I_I, & \text{for} \quad DT < t \le T \end{cases}. \tag{5.65}$$

The RMS value of the current through the diode is found to be

$$I_{D(RMS)} = I_I\sqrt{1-D}. \tag{5.66}$$

Using (5.24), $I_{D(RMS)}$ can be expressed in terms of I_O as

$$I_{D(RMS)} = \frac{(1-D)^{\frac{3}{2}}}{(1-2D)^2} I_O. \tag{5.67}$$

The conduction loss in the diode forward resistance R_F is

$$P_{RF} = I^2_{D(RMS)} R_F = \frac{(1-D)^3}{(1-2D)^2} I_O^2 R_F$$

$$= \frac{(1-D)^3 R_F}{(1-2D)^2 R_L} P_O. \tag{5.68}$$

The average value of the diode current is

$$I_D = I_I(1-D) = \frac{(1-D)^2}{(1-2D)} I_O. \tag{5.69}$$

The power loss associated with the forward voltage drop V_F of the diode D is

$$P_{VF} = V_F I_D = \frac{(1-D)^2}{(1-2D)} I_O$$

$$= \frac{(1-D)^2 V_F}{(1-2D) V_O} P_O. \tag{5.70}$$

Using (5.68) and (5.70), the overall power loss in the diode is

$$P_D = P_{VF} + P_{RF} = \Big[\frac{(1-D)^3 R_F}{(1-2D)^2 R_L} + \frac{(1-D)^2 V_F}{(1-2D) V_O} \Big] P_O. \tag{5.71}$$

Power loss in inductors is segregated into core loss and winding loss. Typically for PWM converters the core loss is negligible. The winding loss is dependent on the winding resistance and the RMS value of the current flowing through it. The RMS value of the currents through the Z-network inductors L is approximated to be

$$I_{L(RMS)} = I_I = \frac{1-D}{1-2D} I_O, \tag{5.72}$$

resulting in a power loss given by

$$P_{r_L} = 2 {I_{L(RMS)}}^2 r_L = 2 \Big(\frac{1-D}{1-2D} \Big)^2 \frac{r_L P_O}{R_L}. \tag{5.73}$$

It should be noted that expression (5.73) is multiplied by two since there are two Z-network inductors. The current through the Z-network capacitor C is

$$i_C = \begin{cases} -I_I, & \text{for} \quad 0 < t \leq DT \\ I_I - I_O, & \text{for} \quad DT < t \leq T \end{cases}. \tag{5.74}$$

Using (5.24) and (5.74), the RMS current through C is found to be

$$I_{C(RMS)} = \frac{\sqrt{D(1-D)}}{1-2D} I_O. \tag{5.75}$$

The power loss associated with the Z-network capacitors C is

$$P_{rC} = 2{I_{C(RMS)}}^2 r_C = 2\frac{D(1-D)r_C}{(1-2D)^2 R_L} P_O. \tag{5.76}$$

The RMS value of the current through the filter inductor L_f can be approximated to be

$$I_{L_f(RMS)} = I_O. \tag{5.77}$$

Power loss in the filter inductor given by

$$P_{r_{LO}} = I_O^2 r_{LO} = \frac{r_{L_f}}{R_L} P_O. \tag{5.78}$$

Using (5.35), (5.44), (5.9), and (5.17), the RMS value of the current through the filter capacitor C_f is

$$I_{C_f(RMS)} = \frac{\Delta i_{L_f}}{\sqrt{12}} = \frac{(V_O - V_I)(1-D)}{L_f f_s \sqrt{12}}. \tag{5.79}$$

The power loss in the filter capacitor is

$$P_{R_{CO}} = {I_{C_f(RMS)}}^2 r_{C_f} = \frac{(V_O - V_I)^2 (1-D)^2}{12{f_s}^2 {L_f}^2} r_{C_f}. \tag{5.80}$$

Using (5.23) and (5.80), the power loss in C_f in terms of the output power is found to be

$$P_{R_{CO}} = \frac{(M_{VDC} - 1)^2 (1-2D)^2 R_L r_{C_f}}{12{f_s}^2 {L_f}^2} P_O. \tag{5.81}$$

Hence, from (5.64), (5.71), (5.73), (5.76), (5.78), and (5.80), the total losses in the PWM Z-source dc-dc converter is

$$P_{loss} = P_{FET} + P_D + P_{r_L} + P_{r_C} + P_{r_{LO}} + P_{r_{CO}}. \tag{5.82}$$

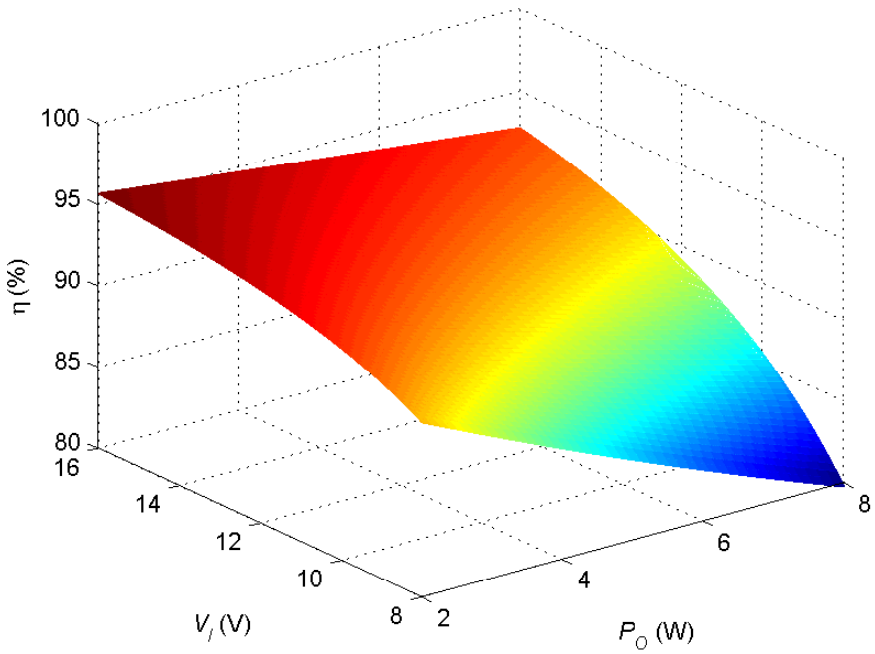

Figure 5.10: Predicted efficiency η as a function of V_I and P_O.

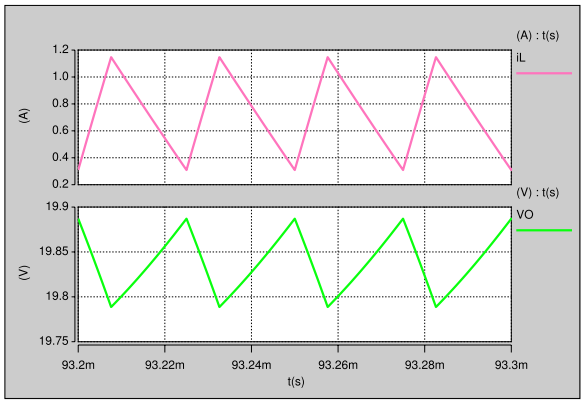

Figure 5.11: Simulated inductor current i_L and output voltage V_O for $D = 0.3$ and $L = 175$ μH.

5.4.2 DC Voltage Conversion Factor of Non-Ideal PWM Z-source dc-dc Converter in CCM

The efficiency of the PWM Z-source dc-dc converter is

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = \frac{1}{1 + \frac{P_{loss}}{P_O}}. \tag{5.83}$$

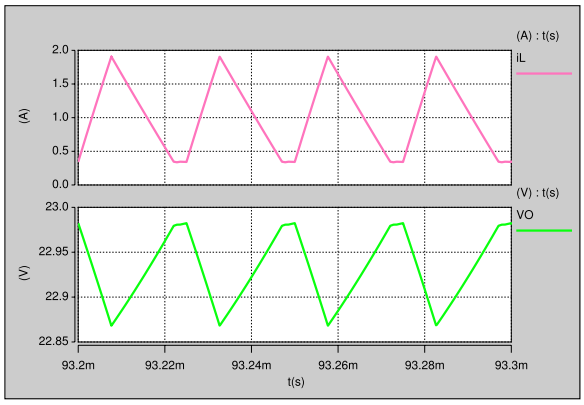

Figure 5.12: Simulated inductor current i_L and output voltage V_O for $D = 0.3$ and $L = 107.5$ μH.

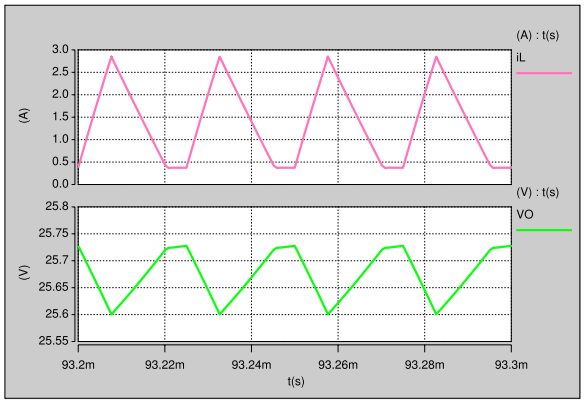

Figure 5.13: Simulated inductor current i_L and output voltage V_O for $D = 0.3$ and $L = 75$ μH.

Using (5.23), (5.24), and (5.83), we obtain

$$\eta = M_{VDC}\frac{1-2D}{1-D}, \tag{5.84}$$

$$M_{VDC(non-ideal)} = \frac{1}{1+\frac{P_{loss}}{P_O}}\frac{1-D}{1-2D}, \tag{5.85}$$

$$M_{VDC(non-ideal)} = \frac{1}{1+\frac{P_{loss}}{P_O}}M_{VDC}. \tag{5.86}$$

In (5.86), M_{VDC} is the dc input-to-output voltage conversion factor for an ideal converter, and P_{loss} is (5.82).

5.5 Experimental and Simulation Results

An example PWM Z-source dc-dc converter with the specifications $V_I = 12$ V, $f_s = 40$ kHz, $L = 330$ μH, $C = 220$ μF, $R_L = 50$ Ω, $L_f = 330$ μH, $C_f = 470$ μF is selected. The inductors (L and L_f) are 1433428C manufactured by Murata Power Solutions with a measured dc resistance $r_L = 0.42$ Ω. The capacitors (C and C_F) are electrolytic capacitors with measured dc resistances of $r_C = 0.22$ Ω and $r_{C_f} = 60$ mΩ, respectively. International Rectifier Power MOSFET IRF520 which is rated for 9.2A/100V and has a maximum $r_{DS} = 0.27$ Ω and $C_O = 150$ pF, and a ON Semiconductor manufactured SWITCHMODE Power Rectifier MBR10100 rated for 10A/100V and having $V_F = 0.65$ V and $R_F = 0.2$ Ω are selected. For the example considered, from (5.33), the minimum value of inductance to ensure CCM operation is

$$L > L_{min} = 0.0858\frac{R_L}{f_s} = 107.25 \ \mu\text{H}. \tag{5.87}$$

From (5.53), the minimum value of filter capacitance beyond which the voltage ripple across the filter capacitor is dependent only on the value of the ESR of C_f is determined to be

$$C_f > \frac{1 - D_{min}}{2 f_s r_{C_f}} = 187.5 \ \mu\text{F}, \tag{5.88}$$

where $D_{min} = 0.1$. It should be noted that the selected values of $L = 330$ μH and $C_f = 470$ μF are in agreement with (5.87) and (5.88), respectively.

Fig. 5.10 shows the variation of predicted efficiency η as a function of V_I and P_O for a fixed $V_O = 20$ V. The parameters used to obtain Fig. 5.10 are as specified by the considered example.

The above PWM Z-source dc-dc converter was simulated in Saber circuit simulator. The parasitics of the passive components were included and the simulation

models of IRF510 and MBR10100 present in the Saber library were employed. Transient simulation was carried out for three different values of L: $L > L_{min} = 175$ μH, $L = L_{min} = 107.25$ μH, and $L < L_{min} = 75$ μH. It can be inferred from Figs. 5.11, 5.12, and 5.13 that for $L > L_{min} = 175$ μH the Z-source dc-dc converter is in CCM, for $L = L_{min} = 107.25$ μH the Z-source dc-dc converter is at the CCM/DCM boundary, and for $L < L_{min} = 75$ μH the Z-source dc-dc converter is in DCM, respectively. The peak-to-peak inductor current predicted by (5.4) is in good agreement with the simulated peak-to-peak inductor current shown in Fig. 5.11, which corresponds to CCM operation. A laboratory prototype was built corresponding to the example. The PWM Z-source dc-dc converter was setup to operate in a open-loop configuration. IR2110, a high-side MOSFET driver was employed to drive the MOSFET. The duty ratio D was varied from $D = 0.1$ to $D = 0.375$ in steps of $\Delta D = 0.025$. Figs. 5.14, 5.15, and 5.16 present the theoretically predicted and experimentally measured V_O, M_{VDC}, and η respectively. The difference in the measured and predicted output voltage V_O, M_{VDC}, and η at higher duty ratios ($D > 0.3$) can be attributed to the losses in the converter due to ringing in the MOSFET and non-idealities in the setup (stray inductances and capacitances) which have not been included in the analysis.

Table 5.1: Theoretical and experimental results

Parameter/Expression	Predicted Value	Measured Value
V_C:(5.22) and (5.86)	16.34 V	16.2 V
v_L:(5.1) and (5.10)	16.34 V and -4.34 V	16.00 V and -4.6 V
v_{L_f}:(5.5) and (5.13)	-16.34 V and 4.34 V	-16.00 V and 4.6 V
Δi_L:(5.4)	309.5 mA	310 mA
Δi_{L_f}:(5.9)	309.5 mA	312.5 mA
$v_{C_f(p-p)}$:(5.55)	18.6 mV	18.7 mV

Table 5.1 presents the theoretically predicted and experimentally measured values of key parameters corresponding to the steady-state analysis. $v_{C_f(p-p)}$ is obtained by measuring Δi_{C_f} to obtain $v_{C_f(p-p)} = \Delta i_{C_f} r_{C_f}$. The parameters correspond to the example considered. Tektronix P6021 AC current probe with a conversion factor of 2 mA/mV was employed to obtain the current measurements. Fig. 5.17 shows the

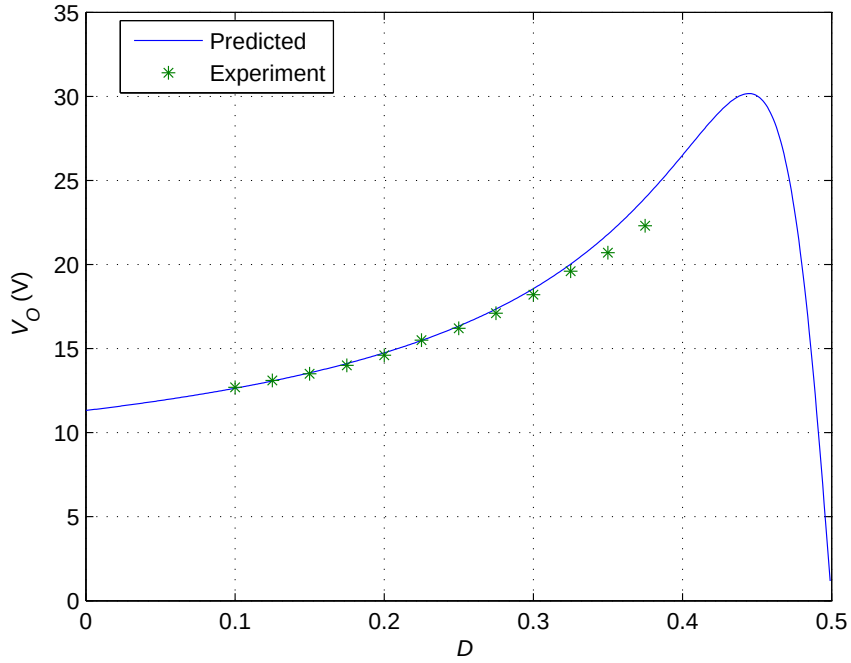

Figure 5.14: V_O as s function of D for $V_I = 12$ (V) .

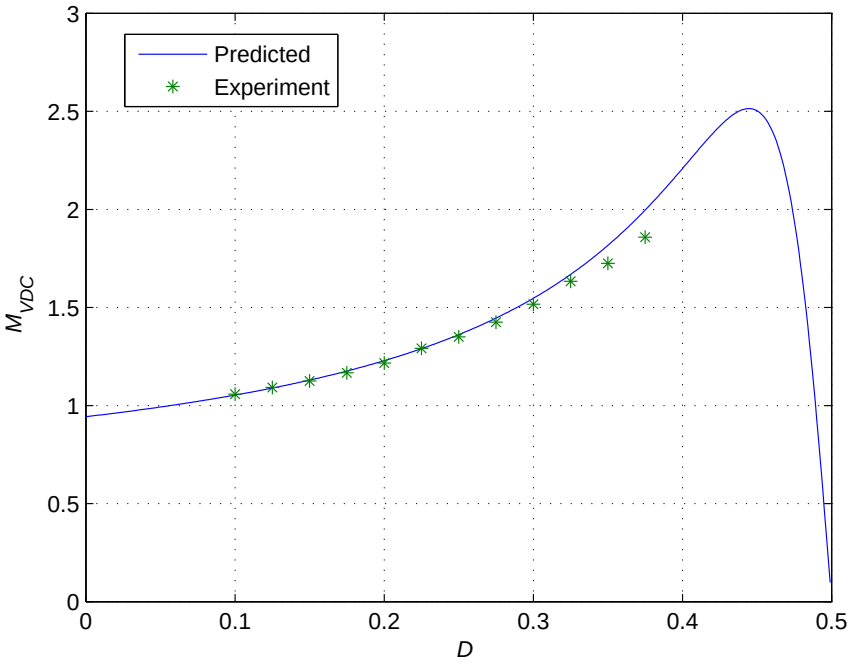

Figure 5.15: M_{VDC} as s function of D for $V_I = 12$ (V).

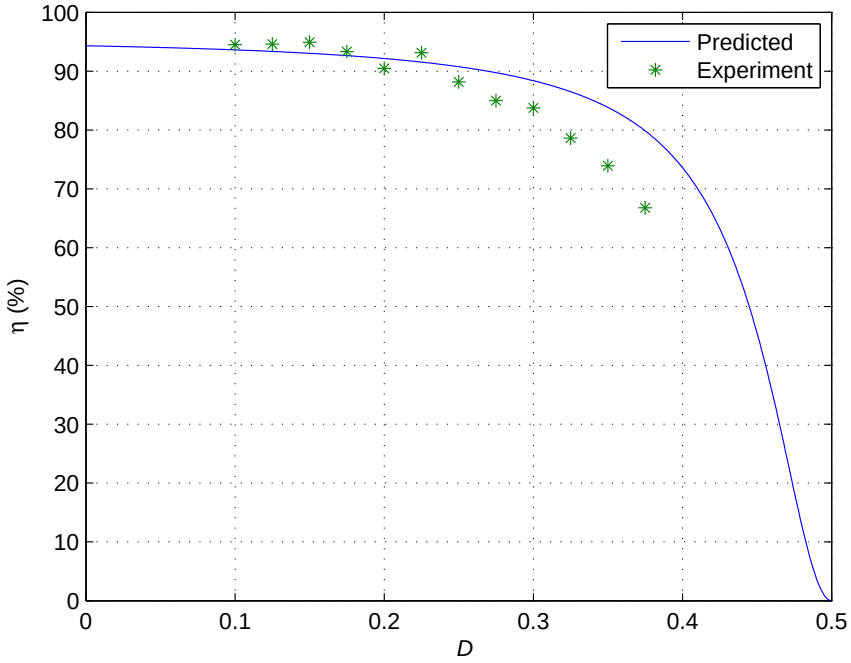

Figure 5.16: η as a function of D for $V_I = 12$ (V).

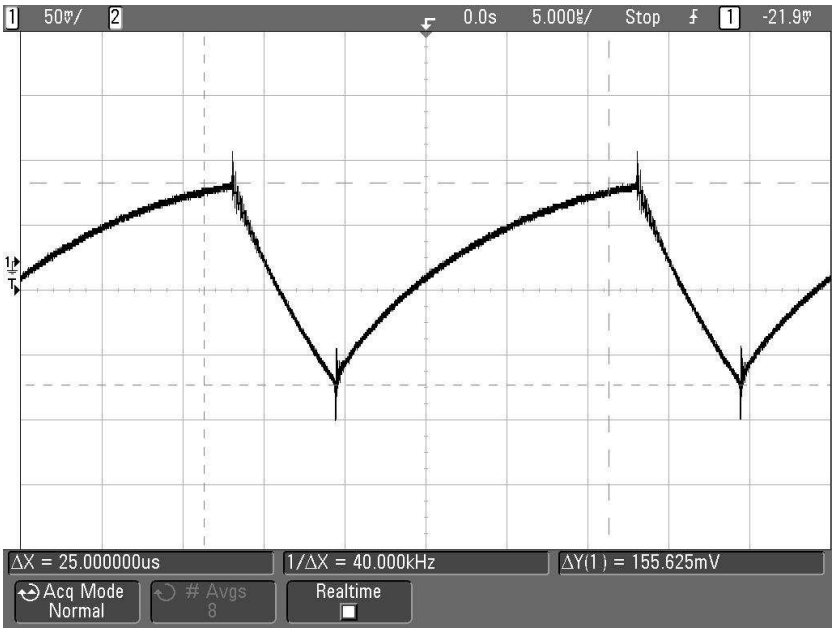

Figure 5.17: Current through the filter capacitor i_{C_f}: 2 mA/mV.

Figure 5.18: Experimental waveforms- Upper trace: Differential probe scaling 20:1, v_{GS} 1 V/div. Lower trace: i_L measured across 1Ω sense resistor 500 mV/div and 1 mA/1 mV.

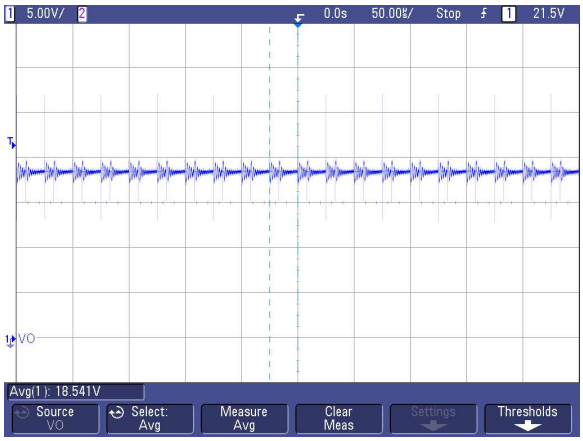

Figure 5.19: Experimental steady-state output voltage V_O for $V_I = 12$ V and $D = 0.3$.

current waveform through C_f obtained for $D = 0.25$. Differential probe master 4231 was employed to obtain the pulsating voltage measurements.

Fig. 5.18 shows the waveforms of v_{GS} and i_L of for the PWMMZ-source dc-dc converter operating in CCM. v_{GS} was measured using a differential probe: Probe Master 4231 with a scaling factor of 20:1. The inductor current waveform was obtained by measuring the voltage across a sense resistor of 1 Ω connected in series with L. Fig. 5.19 shows the steady-state output voltage for $D = 0.3$ and $V_I = 12$ V. The Agilent DS05012A oscilloscope was used to record the waveforms.

6 Conclusions

6.1 Small-Signal Modeling of PWM Z-Source Converter for CCM

The large-signal averaged model, dc, and ac small-signal linear model of the power-stage of PWM Z-source converter operating in CCM have been derived. The non-linear, disjoint PWM switch of the PWM Z-source converter has been approximated by an averaged linear model by using circuit-averaging technique. Small-signality conditions that have to be satisfied for the model to be linear have been deduced and presented. Power-stage input voltage-to-capacitor voltage, input voltage-to-inductor current, control-to-capacitor voltage, and control-to-inductor current transfer functions have been derived. The transfer functions take into account the ESRs of the inductors and the capacitors. An example PWM Z-source converter was considered, and the associated Bode plots were predicted using the derived transfer functions. Measured values of ESRs of the inductors and capacitors were used in obtaining the theoretical Bode plots. A laboratory prototype was built, and the input voltage-to-capacitor voltage, input voltage-to-inductor current, and control-to-capacitor voltage, and control voltage-to-inductor current transfer functions were measured using HP4194A Gain-Phase Analyzer. The theoretically predicted step-responses were found to be in good agreement with the experimental step-responses. The theoretically predicted and the experimentally obtained Bode plots were in good agreement even at the high frequency region, thereby validating the derived small-signal models.

6.2 Steady-State Analysis of PWM Z-Source dc-dc Converter for CCM

A detailed steady-state analysis of PWM Z-source dc-dc converter operating in CCM has been presented. The dc input-to-output voltage conversion factor for an ideal PWM Z-source dc-dc converter has been derived. Equations for power loss in each

of the components of the PWM Z-source dc-dc converter have been derived. Based on the power loss expressions derived, expressions for the overall efficiency and the dc voltage conversion factor of a non-ideal PWM Z-source dc-dc converter are determined. The minimum Z-network inductance L required to ensure CCM operation has been derived. The output voltage ripple due to C_f and r_{C_f} have been analyzed, and the derivation of expressions to determine the same are presented. A laboratory prototype was built to verify the theoretical analyses. The predicted output voltage V_O was in good agreement with the experimental results for discrete points of duty ratio D from $D = 0.1$ to $D = 0.35$ as shown in Fig. 5.14. The predicted efficiency was in good agreement with experimental results for discrete points of duty ratio D from $D = 0.1$ to $D = 0.3$. However, a discrepancy was noticed for D beyond 0.3, as shown in Fig. 5.16. This can be due to the fact that the losses due to high-frequency ringing of the MOSFET have not been considered. The predicted output voltage ripple was also in good agreement with the experimentally measured ripple as shown in Table I and Fig. 5.17. The disadvantage of the PWM Z-source dc-dc converter as compared to conventional boost converter topology is its higher part count. However, the merits of the PWM Z-source dc-dc converter are:

- For the same duty ratio D and input voltage V_I, PWM Z-source dc-dc converter offers a higher output voltage.

- Since the diode is turned OFF when the MOSFET is ON, if there is a short on the load side, the source is isolated from the load. This provides inherent immunity to disturbances at the load side. This can be critical if the fuel or energy source is expensive and is to be protected.

- Since the input-to-output voltage conversion factor is $M_{VDC} = \frac{1-D}{1-2D}$ for $D > 0.5$, the output voltage is inverted. It can be employed, where such a feature is desired

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